

# COMPAL CONFIDENTIAL

MODEL NAME : CDP80/CDP81

PCB NO : LA-E152P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

## Breckenridge 15 DSC (TBT)

Kabylake H

2016-11-10

REV : 1.0 (A00)

@ : Nopop Component

N16@ : N16S-GT1-KA Component

N17@ : N17M-Q3 Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

eSPI@ : eSPI interface

LPC@ : LPC interface

MB PCB

Part Number	Description
DAA000CP010	PCB 15E LA-E152P REV1 MB DSC AR 1

Layout Dell logo



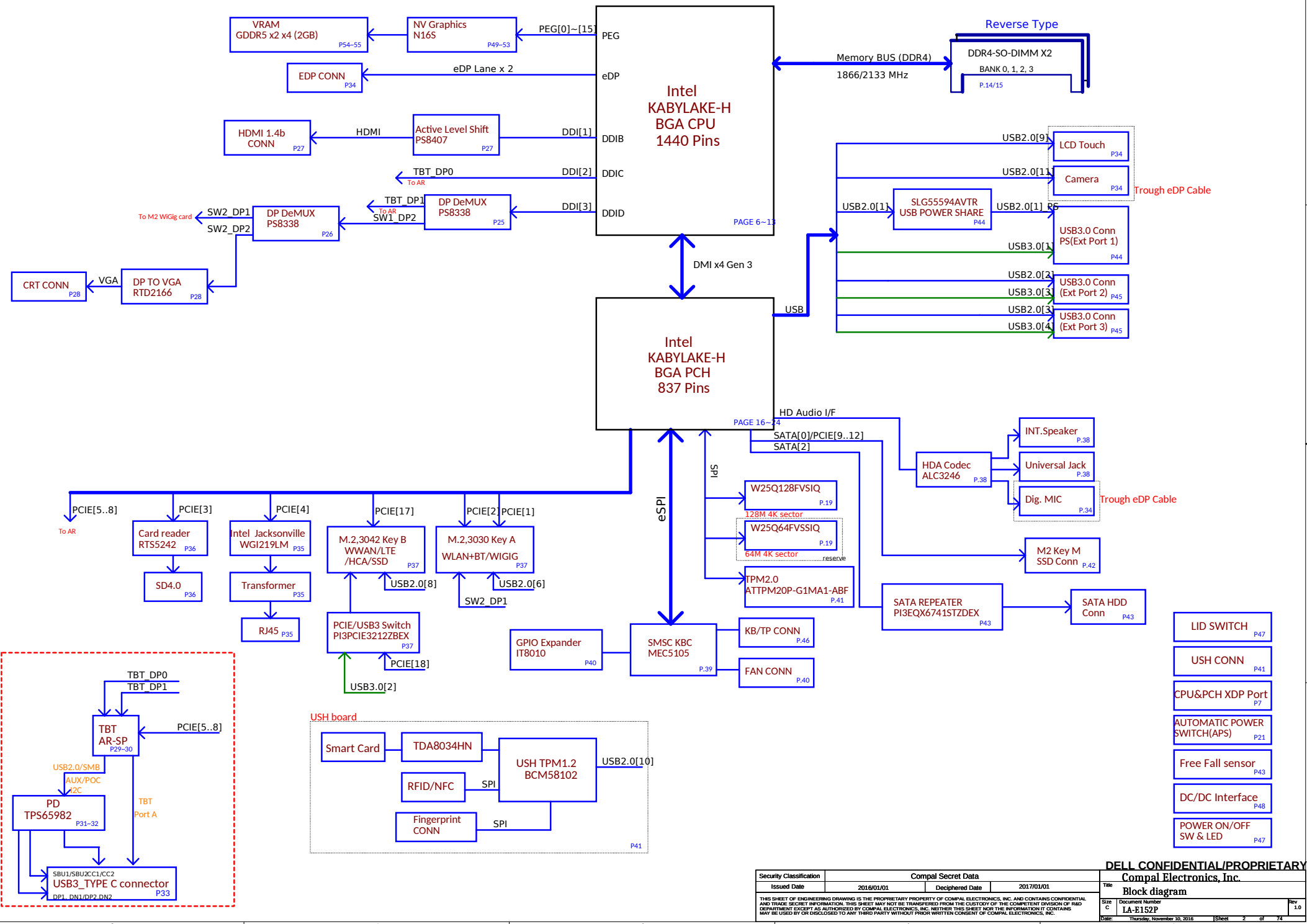
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REV: A00  
PWB: DNY4D

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## Breckenridge 15 DSC TBT Block Diagram





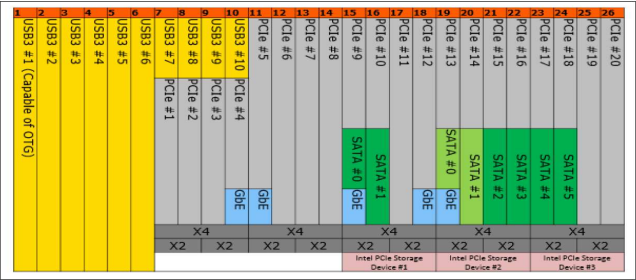
POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	IT-158	0.5
		Add Plating		
Top	3.7	Prepreg	0.5oz+plating	1.6
GND	3.6	Copper foil	1oz	1.25
IN 1	3.6	Copper foil	4mil	4
GND/PWR	3.8	Prepreg	2116H	1.3
IN 2	3.7	Copper foil	1oz	1.25
IN 2	3.7	Copper foil	4mil	4
IN 3	4	Prepreg	1080H x2	1.25
IN 3	3.7	Copper foil	1oz	1.25
GND/PWR	3.8	Prepreg	2116H	1.3
IN 4	3.6	Copper foil	1oz	1.25
GND	3.7	Copper foil	4mil	4
Bottom	3.7	Prepreg	0.5oz+plating	1.6
		Add Plating		
		SolderMask	IT-158	0.5
all Thickness (1.2mm ± 10%)				48.60000



USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Rear
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB1-->Right
USB3.0-4				JUSB2-->Left
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		JNGFF1-->M.2 3030(WIGIG)
USB3.0-8		PCIE-2		JNGFF1-->M.2 3030(WLAN)
USB3.0-9		PCIE-3		Card Reader
USB3.0-10		PCIE-4		LOM
		PCIE-5		Alpine Ridge - SP (pop only on Precision SKU)
		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9	SATA-0A	M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10	SATA-1A	
		PCIE-11		
		PCIE-12		
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB3-->Rear
2	JUSB1-->Right
3	JUSB2 ->Left
4	NA
5	NA
6	JNGFF1--> M.2 3030(BT)
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA

USH	H	BIO
-----	---	-----

VIDEO		DESTINATION
eDP		LCD
DDI-B		JHDMI1
DDI-C		Alpine Ridge - SP (Port 0)
DDI-D	DeMux 1	Alpine Ridge - SP (Port 1)
	DeMux 2	M.2 3030 (WiGig)
		MB VGA

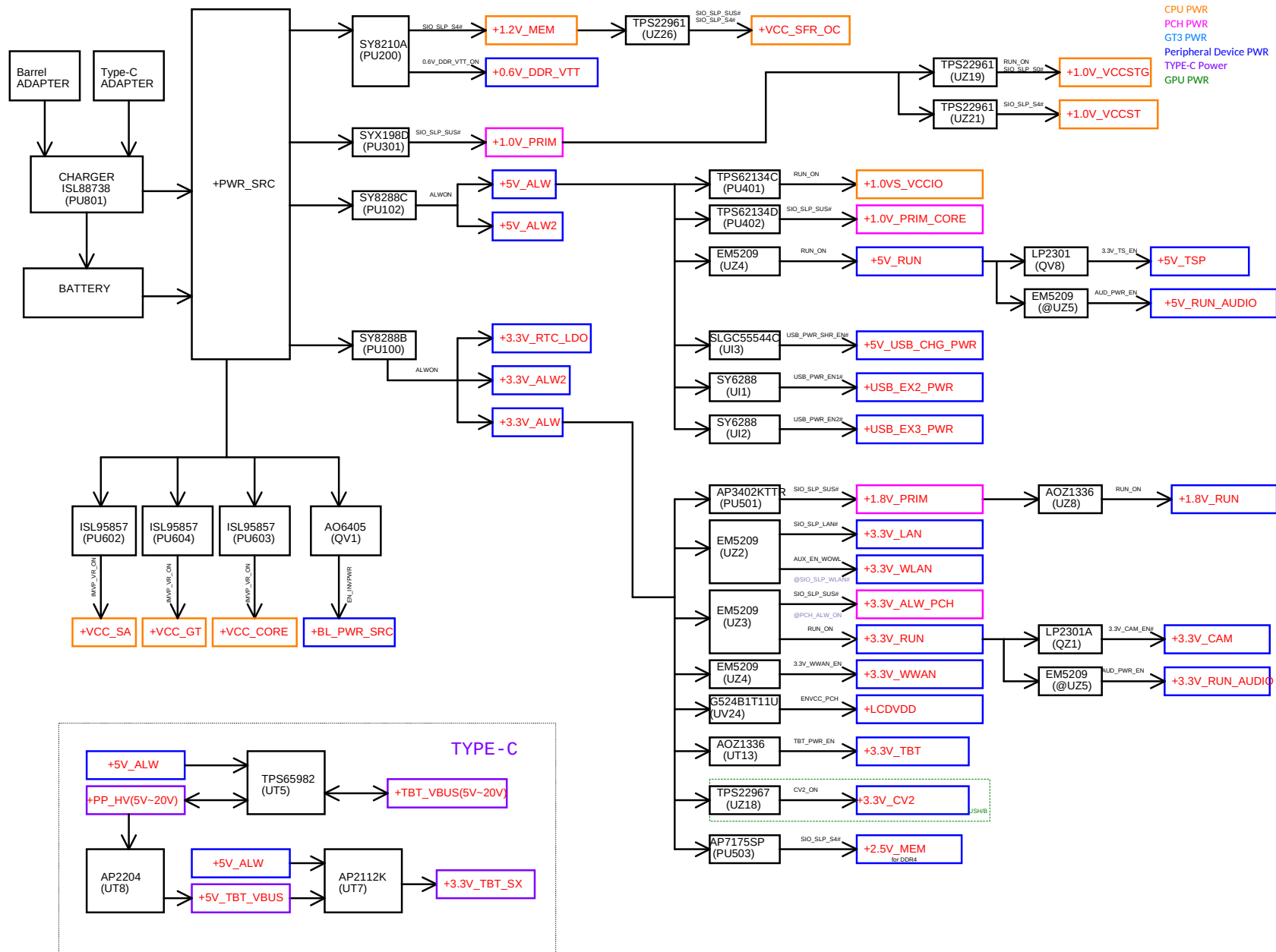
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Port Assignment

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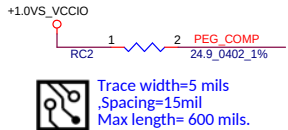




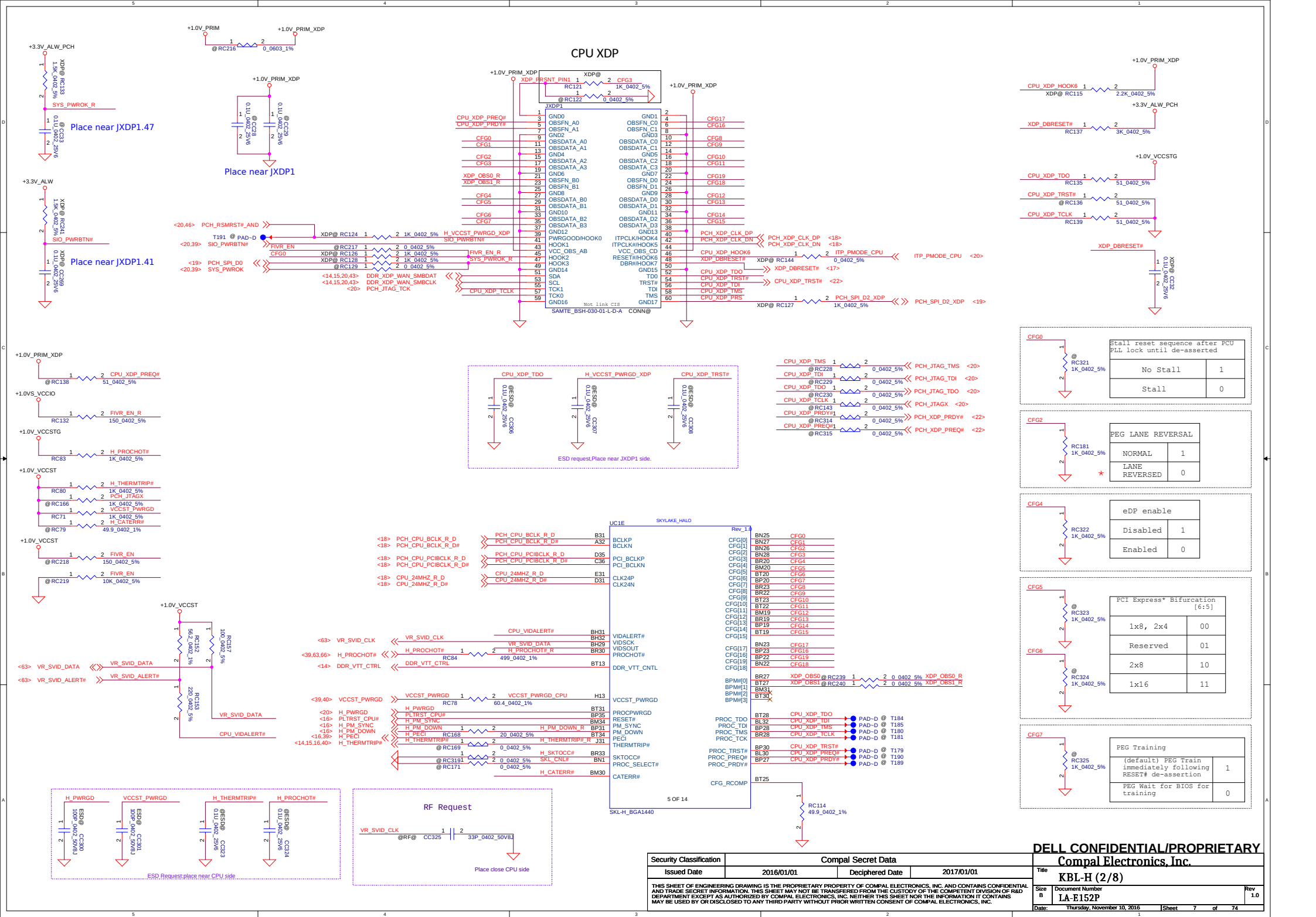




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PEG\_CRX\_GTX\_N[0..15] << PEG\_CRX\_GTX\_N[0..15] <49>  
PEG\_CTX\_C\_GRX\_P[0..15] >> PEG\_CTX\_C\_GRX\_P[0..15] <49>  
PEG\_CTX\_C\_GRX\_N[0..15] >> PEG\_CTX\_C\_GRX\_N[0..15] <49>









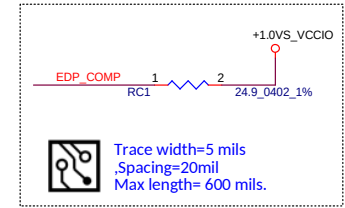
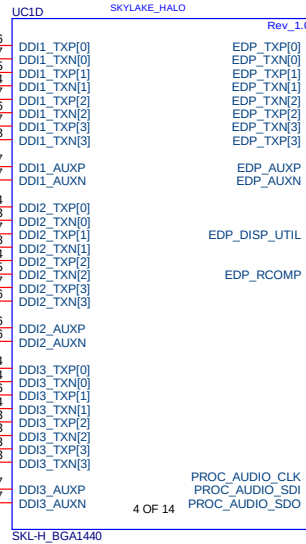




HDMI

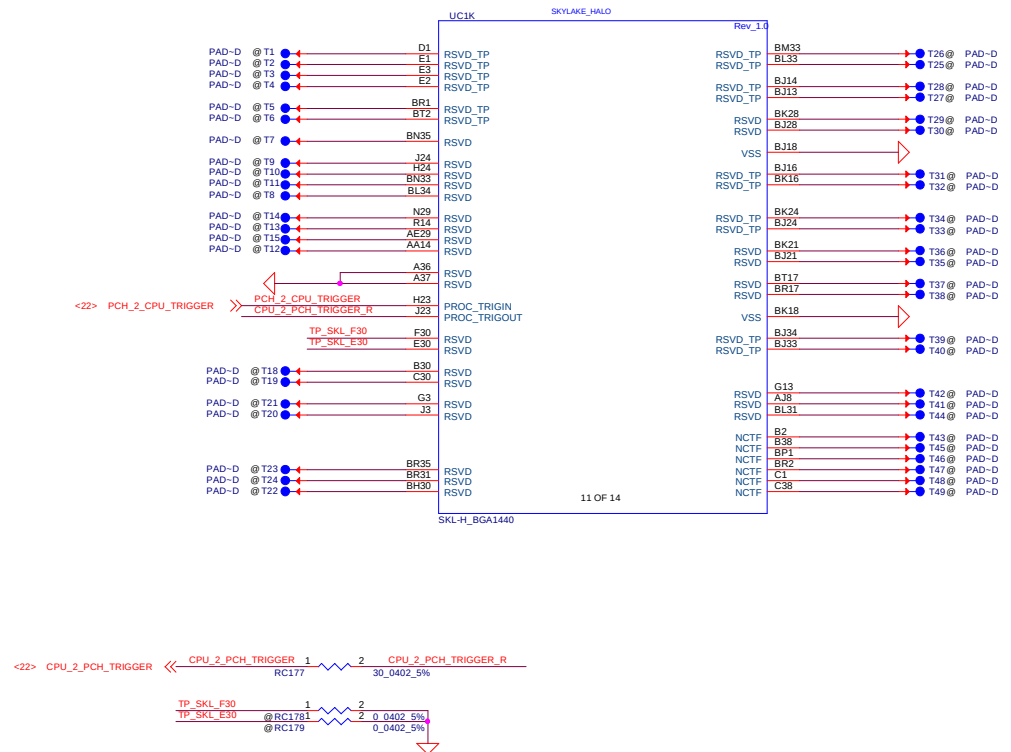
AR P0

AR P1 , WIGIG , VGA



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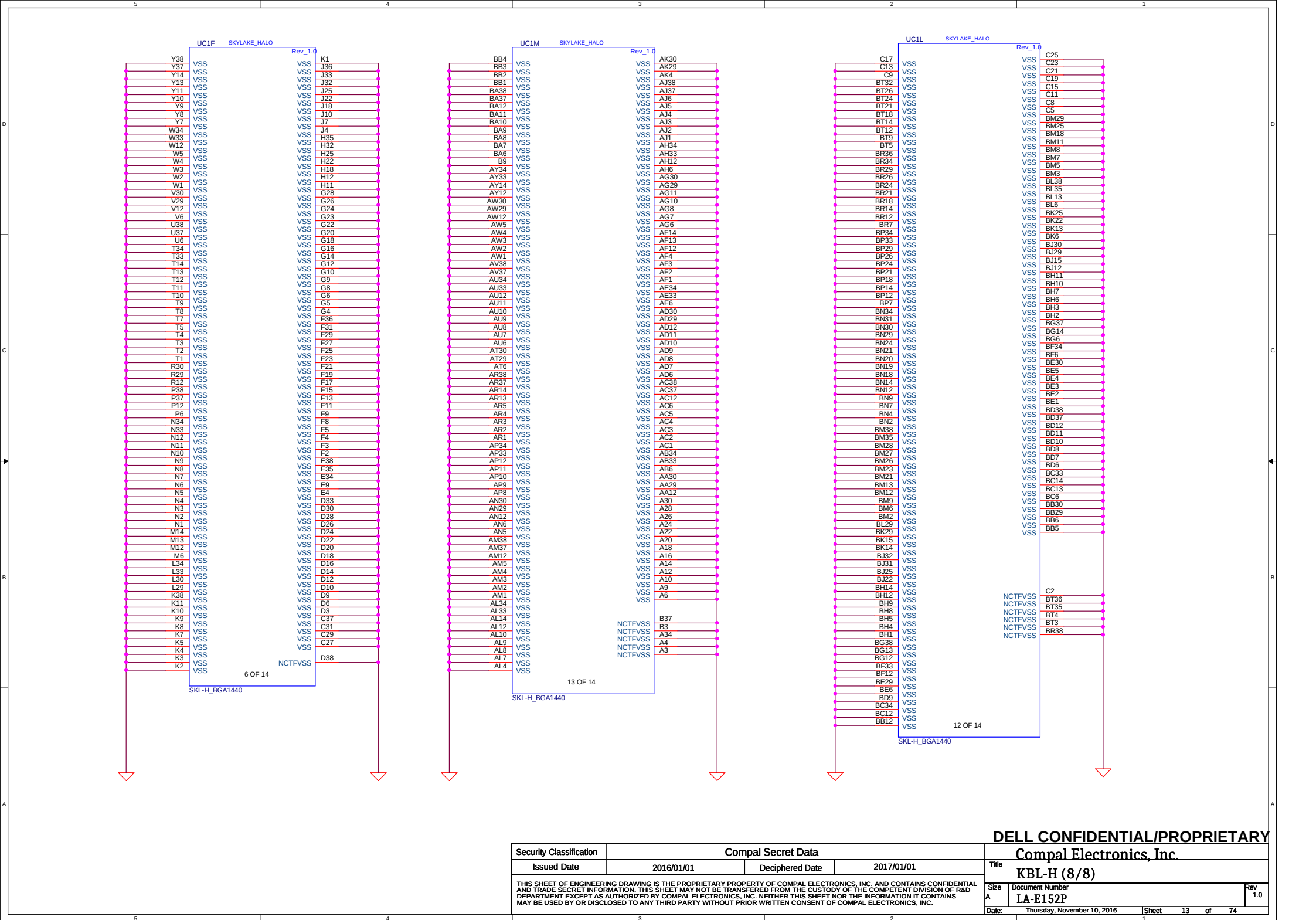












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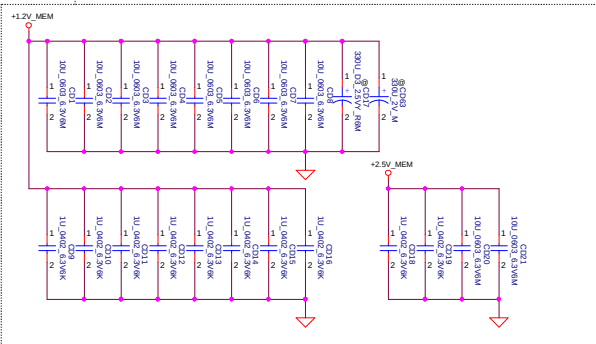
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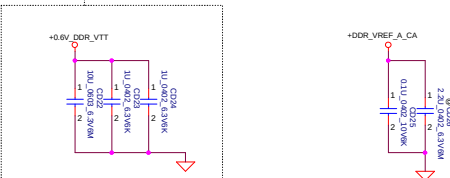


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 <B> DQR\_A\_DQ080\_8I  
 <B> DQR\_A\_DQ080\_8I  
 <B> DQR\_A\_DQ0\_15I  
 <B> DQR\_A\_DQ0\_15I  
 <B> DQR\_A\_DQ0\_15I  
 <B> DQR\_A\_DQ0\_15I  
 <B> DQR\_A\_DQ0\_15I

Layout Note:  
Place near J1MM1



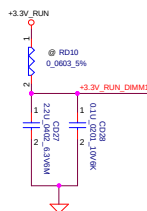
Layout Note:  
Place near J1MM1.258



## DIMM Select

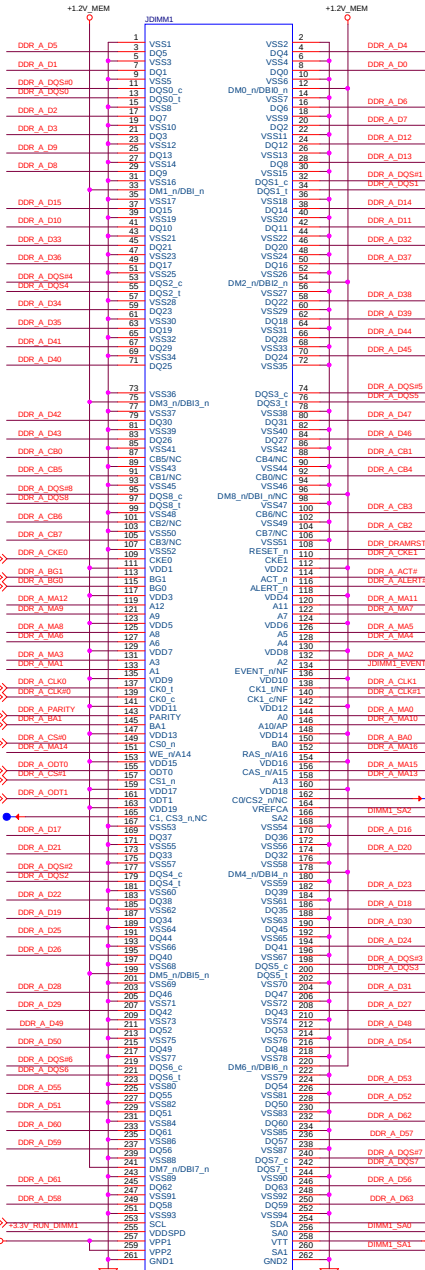
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	1	0
DIMM3	0	1	0
DIMM4	1	1	0

Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

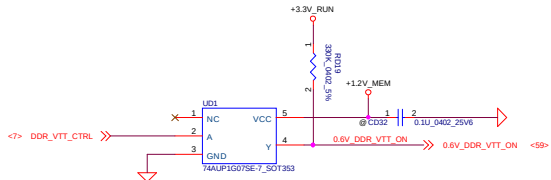
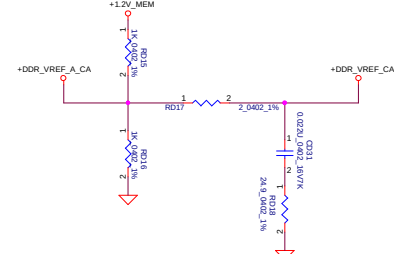
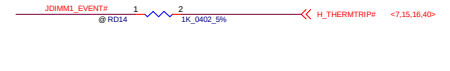
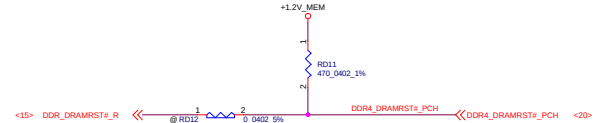


<7,15,20,43> DDR\_XDP\_WAH\_SMBCLK << <7,15,20,43>

+2.5V\_MEM



DDR\_DQ080-Q080-0103  
CONN@



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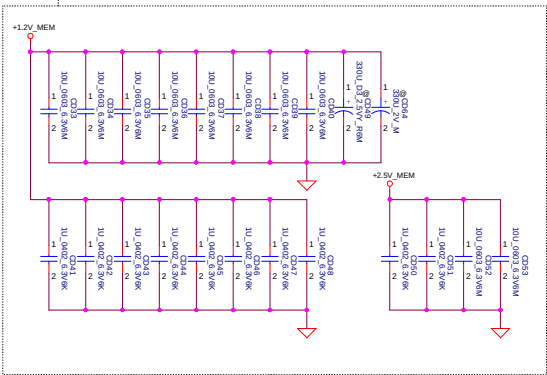
DDR4-SODIMM SLOT1

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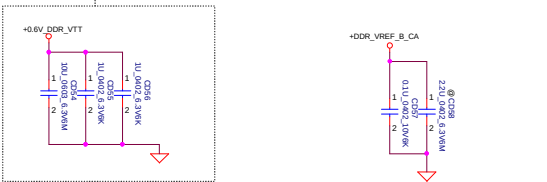


<> DDR\_B\_C0[0..7]  
 <> DDR\_B\_C0[8..15]  
 <> DDR\_B\_C0[16..23]  
 <> DDR\_B\_C0[24..31]  
 <> DDR\_B\_C0[32..39]  
 <> DDR\_B\_C0[40..47]  
 <> DDR\_B\_C0[48..55]  
 <> DDR\_B\_C0[56..63]

Layout Note:  
Place near J1MM2

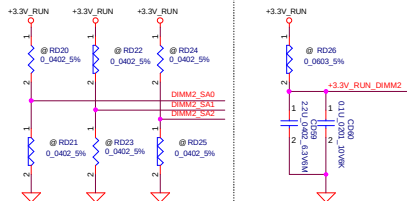


Layout Note:  
Place near J1MM2.258

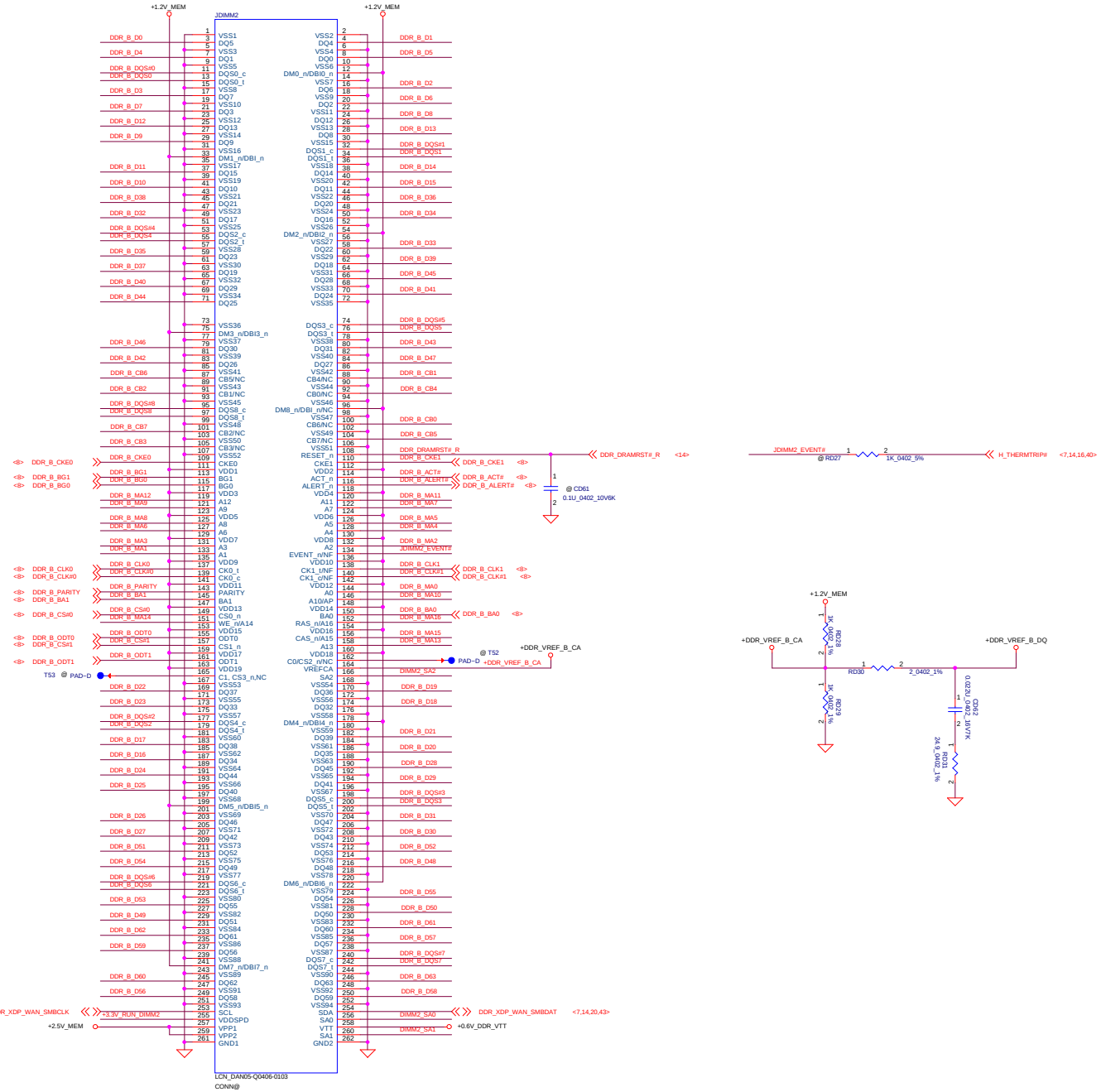


## DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]



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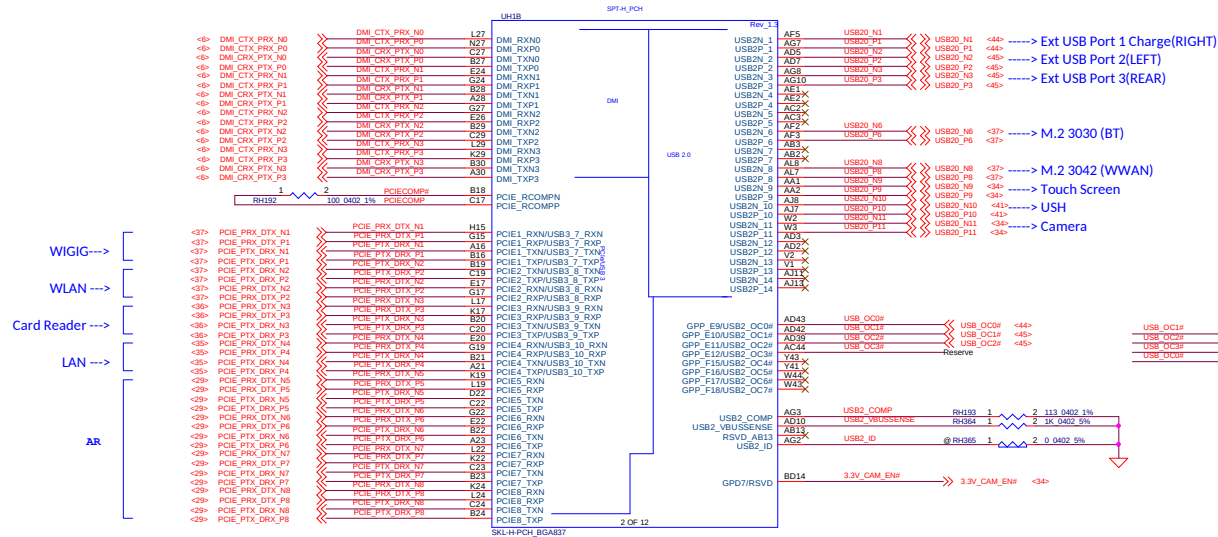
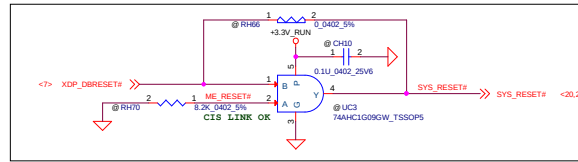
DDR4-SODIMM SLOT2

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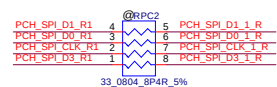
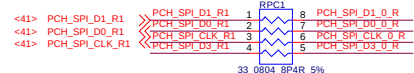
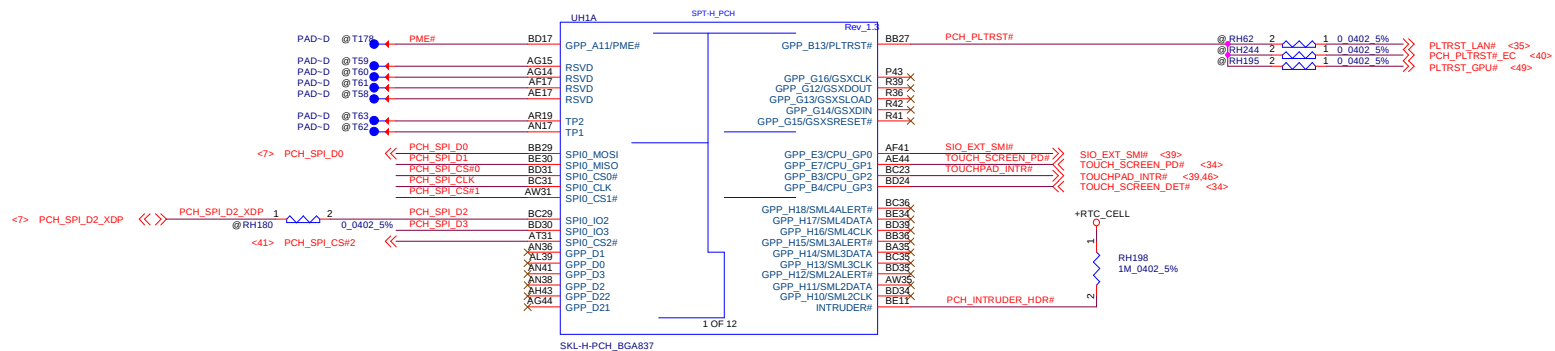
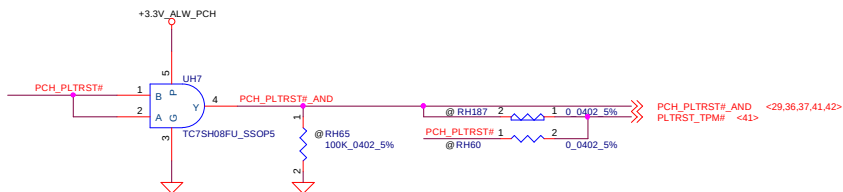
KABYLAKE PCH-H (2/9)

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Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

The schematic diagram illustrates the SPI interface for two flash memory chips: a 128Mb Flash ROM (UC5) and a 64Mb Flash ROM (UC6). Both chips are connected to a common SPI bus. The 128Mb chip is connected to the PCH\_SPI\_CS#0\_R1 pin (RH37) and the PCH\_SPI\_D2\_R1 pin (RH3511). The 64Mb chip is connected to the PCH\_SPI\_CS#1\_R1 pin (RH3521) and the PCH\_SPI\_D2\_R1 pin (RH3531). The SPI bus is connected to a +3.3V SPI supply and a 0.1uF capacitor (CH9) to ground. The chips are also connected to a common ground.

**128Mb Flash ROM (UC5) Pin Connections:**

- PCH\_SPI\_CS#0\_R1 @RH37: 1
- PCH\_SPI\_D2\_R1 RH3511: 2
- PCH\_SPI\_CS#0\_R2: 2
- PCH\_SPI\_D1\_0\_R: 3
- PCH\_SPI\_D2\_0\_R: 3
- PCH\_SPI\_D1\_1\_R: 4
- PCH\_SPI\_D2\_1\_R: 4

**64Mb Flash ROM (UC6) Pin Connections:**

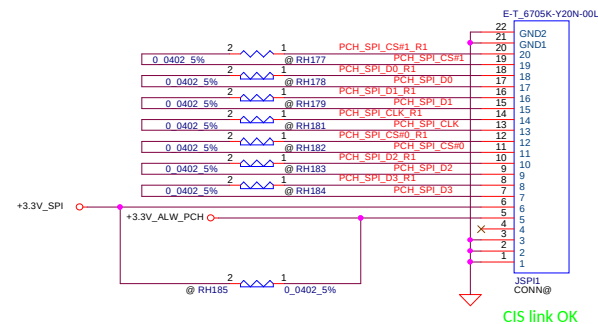
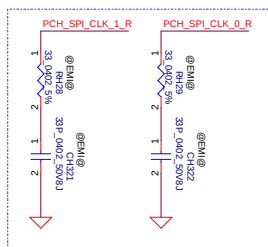
- PCH\_SPI\_CS#1\_R1 @RH3521: 2
- PCH\_SPI\_D2\_R1 RH3531: 2
- PCH\_SPI\_CS#1\_R2: 2
- PCH\_SPI\_D1\_1\_R: 3
- PCH\_SPI\_D2\_1\_R: 3
- PCH\_SPI\_D1\_0\_R: 4
- PCH\_SPI\_D2\_0\_R: 4

**Common SPI Bus Connections:**

- +3.3V SPI
- CH9: 1, 2
- 0.1uF, 0201 10V6K

**Chip Pin Connections:**

- UC5: 1 (VCC), 2 (DQ(0)), 3 (/HOLD(0)), 4 (WP(0)), 5 (GND), 6 (DI(0)), 7 (VCC), 8 (DQ(1)), 9 (/HOLD(1)), 10 (WP(1)), 11 (GND), 12 (DI(1))
- UC6: 1 (VCC), 2 (DQ(0)), 3 (/HOLD(0)), 4 (WP(0)), 5 (GND), 6 (DI(0)), 7 (VCC), 8 (DQ(1)), 9 (/HOLD(1)), 10 (WP(1)), 11 (GND), 12 (DI(1))

Need check

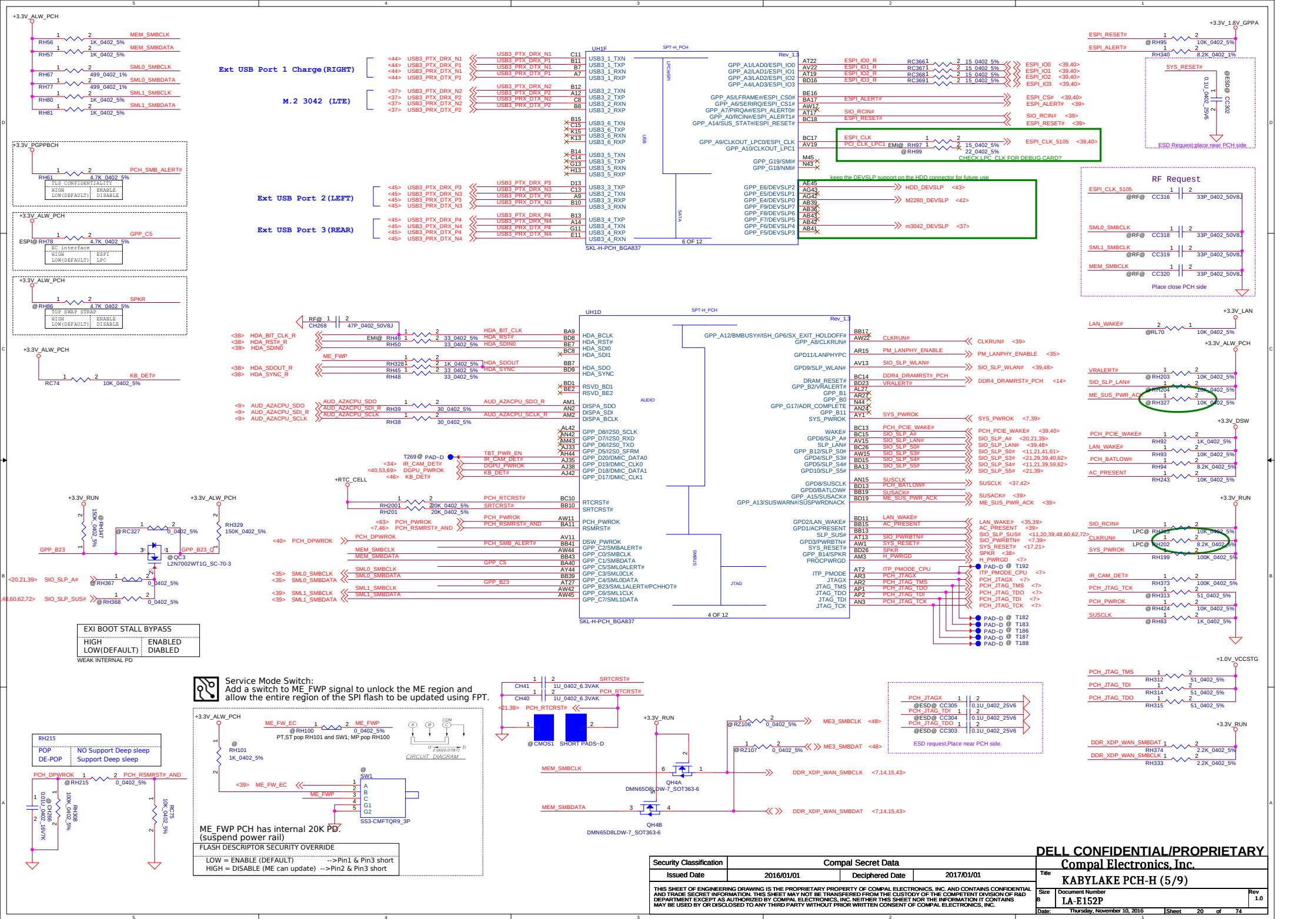
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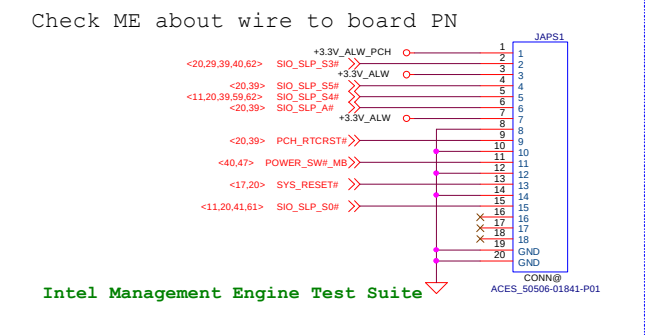
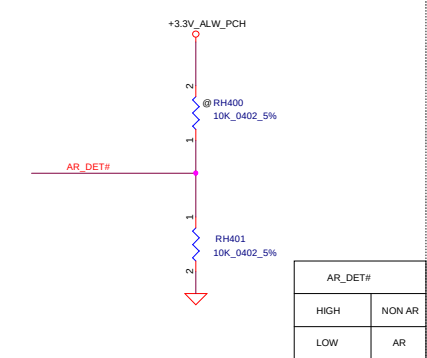
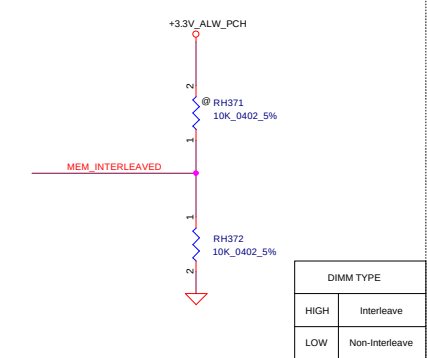
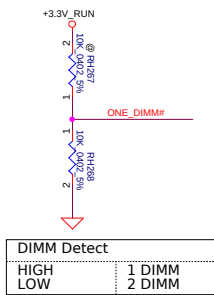
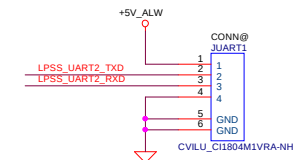
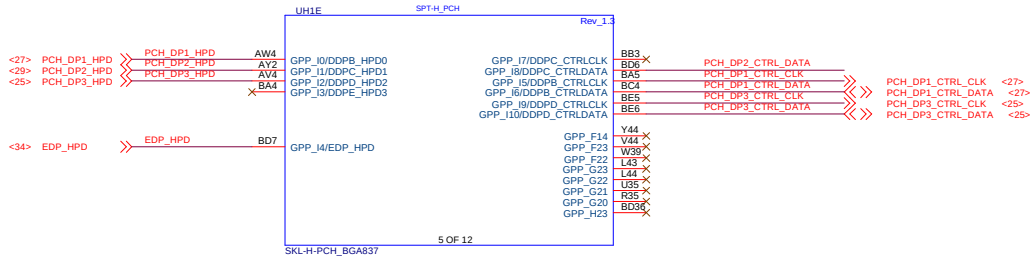
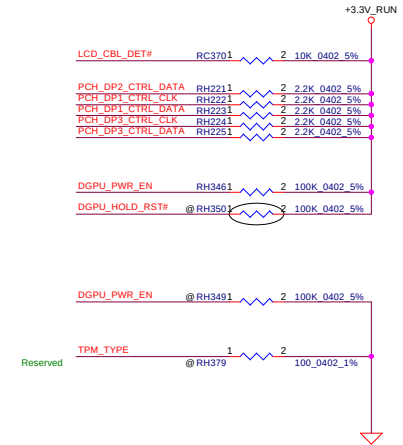
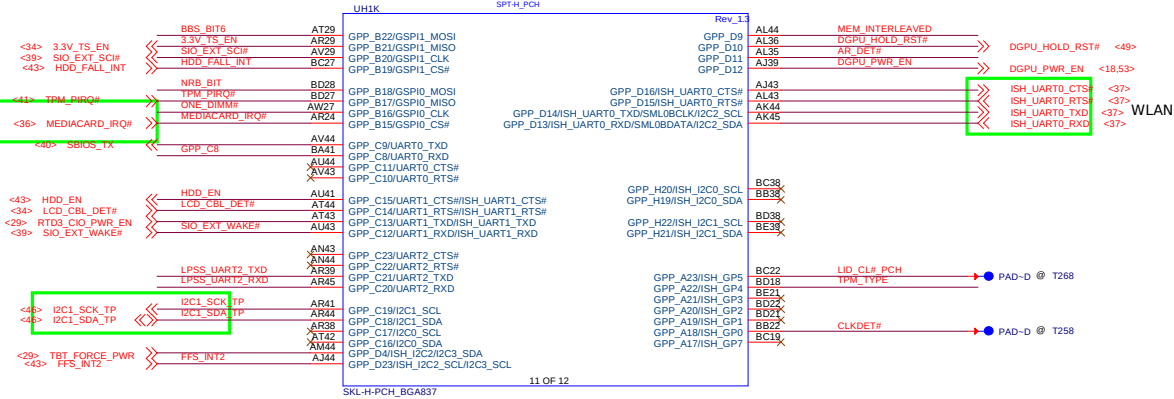
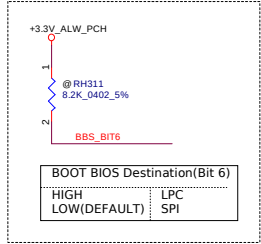
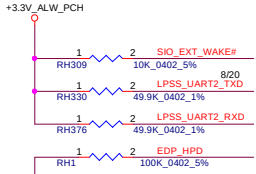
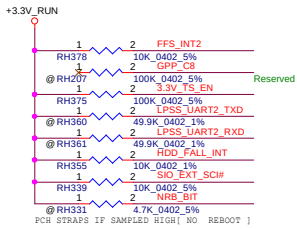
Size	Document Number	Rev
8	IA-E152P	1.0

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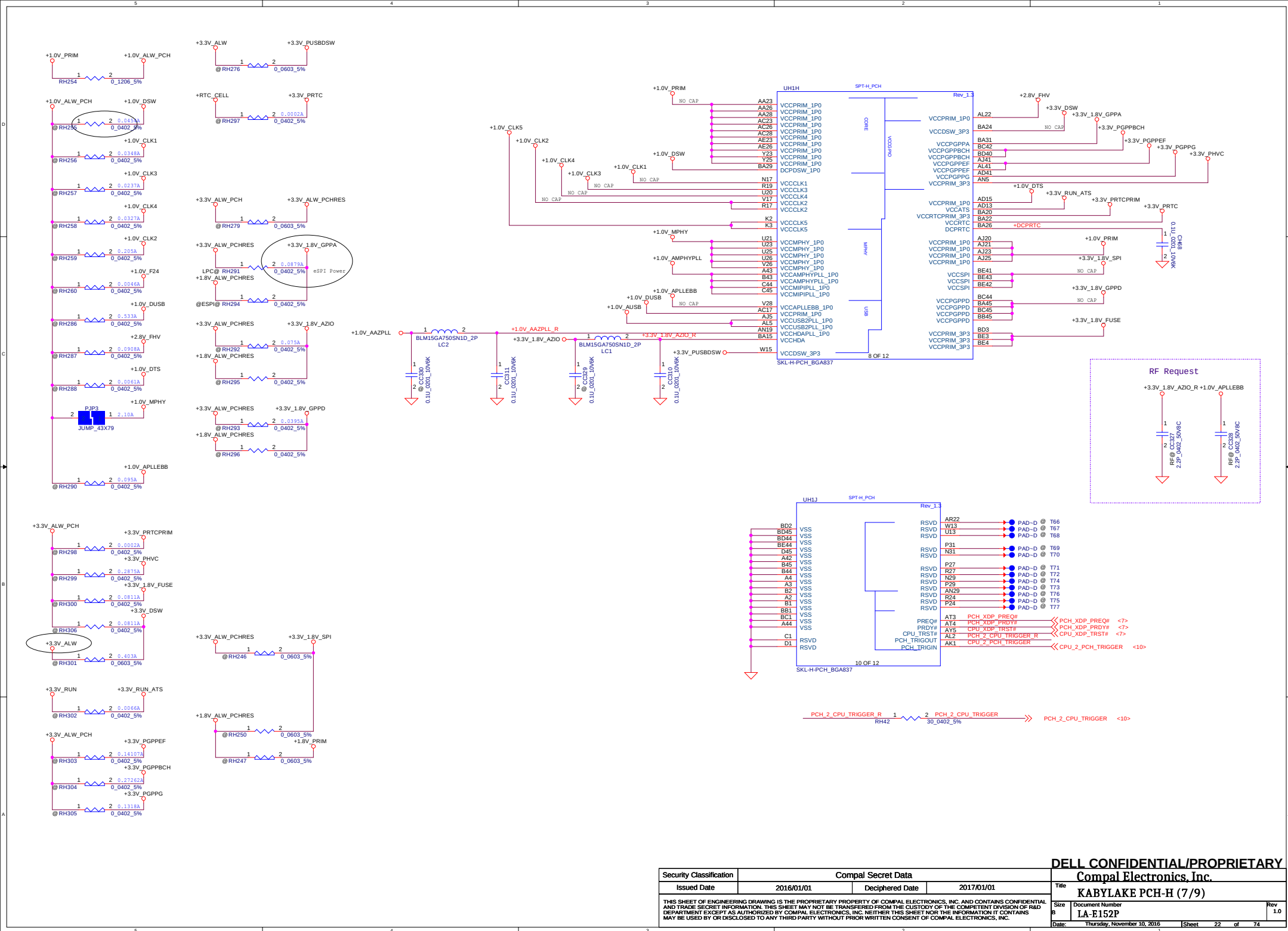




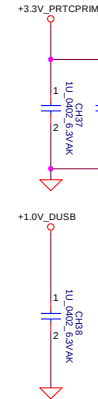
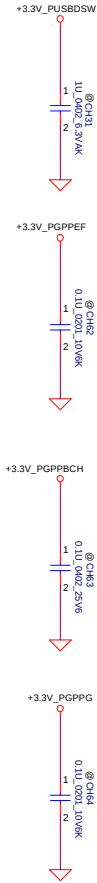
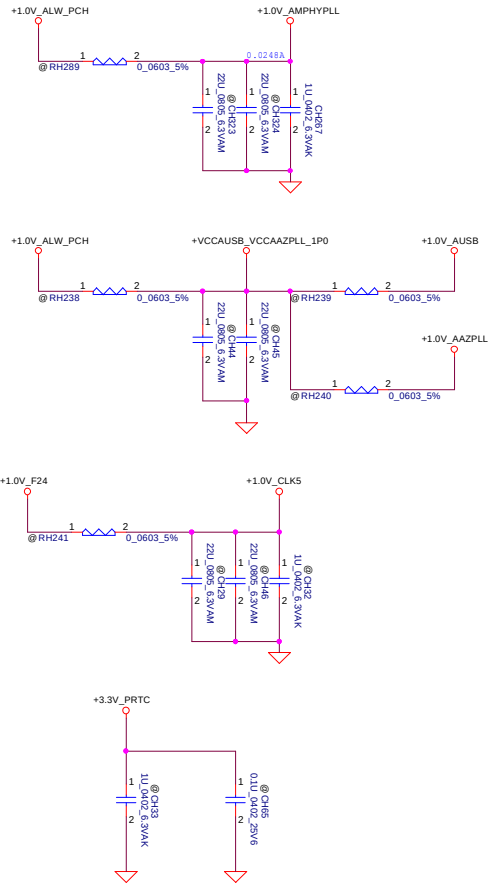












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UJH11 SPT-H\_PCH  
Rev. 1.3

AC18	VSS	AR5
AN4	VSS	AR7
AN10	VSS	U15
BE14	VSS	AL4
BE18	VSS	AE29
BE23	VSS	AE4
BE28	VSS	AE42
BE32	VSS	AF18
BE37	VSS	AF20
BE40	VSS	AF21
BE9	VSS	AF23
C10	VSS	AF25
C2	VSS	AF26
C28	VSS	AF28
C37	VSS	AF29
J7	VSS	AG11
K10	VSS	AG13
K27	VSS	AG31
K33	VSS	AG32
K36	VSS	AG33
K4	VSS	AG38
K42	VSS	AG4
K43	VSS	AH1
L12	VSS	AH17
L13	VSS	AH18
L15	VSS	AH20
L4	VSS	AH21
L41	VSS	AH23
L8	VSS	AH25
M35	VSS	AH26
M42	VSS	AH28
N10	VSS	AH29
N15	VSS	AH45
N19	VSS	AJ10
N22	VSS	AJ14
N24	VSS	AJ15
N35	VSS	AJ17
N36	VSS	AJ18
N4	VSS	AJ26
N41	VSS	AJ28
N5	VSS	AJ29
P17	VSS	AJ31
P19	VSS	AJ32
P22	VSS	AJ36
P45	VSS	AK4
R10	VSS	AK42
R14	VSS	AL7
R22	VSS	AV17
R29	VSS	AV24
R33	VSS	AV27
R38	VSS	AV31
R5	VSS	AV33
T1	VSS	AV6
T2	VSS	AW13
T4	VSS	AW19
Y18	VSS	AW29
Y20	VSS	AW37
Y21	VSS	AW8
Y26	VSS	AY38
Y28	VSS	AY45
Y29	VSS	B25
A18	VSS	B3
A25	VSS	B37
A32	VSS	B40
A37	VSS	B6
AA17	VSS	BA1
AA18	VSS	BB11
AA20	VSS	BB16
AA21	VSS	BB21
AA25	VSS	BB25
AA29	VSS	BB30
AA4	VSS	BB34
AA42	VSS	Bc2
AB10	VSS	BD43
	VSS	

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SKL-H-PCH\_BGA837

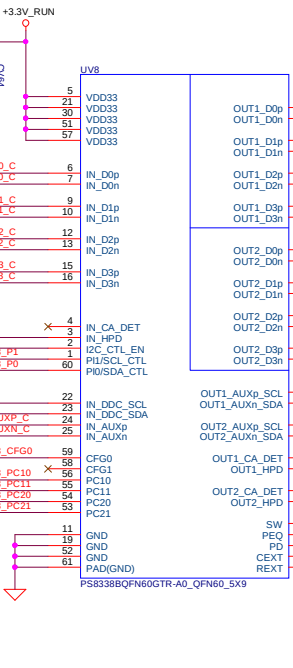
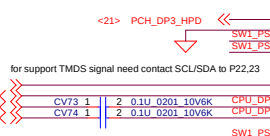
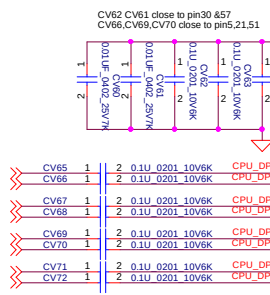
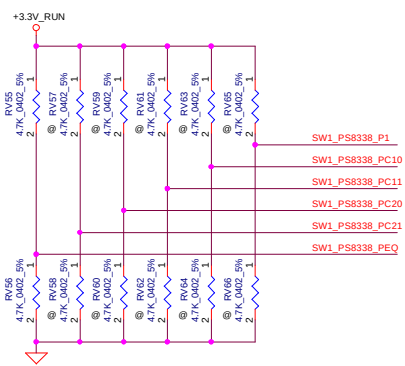
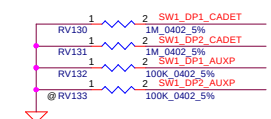
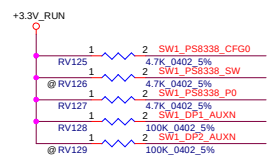
UJH11 SPT-H\_PCH  
Rev. 1.3

C42	VSS	AB11
D10	VSS	AB7
D12	VSS	AB14
D15	VSS	AB31
D16	VSS	AB32
D17	VSS	AB38
D19	VSS	AB4
D21	VSS	AB5
D24	VSS	AC1
D25	VSS	AC20
D27	VSS	AC21
D29	VSS	AC25
D30	VSS	AC29
D31	VSS	AC45
D33	VSS	AB8
D35	VSS	AD11
D36	VSS	AD14
E13	VSS	AB15
E15	VSS	AD32
E31	VSS	AD33
E33	VSS	AD36
F44	VSS	AD4
F8	VSS	AD8
G42	VSS	AE18
G9	VSS	AE20
H17	VSS	AE21
H19	VSS	AE25
H22	VSS	AE28
H24	VSS	AL10
H27	VSS	AL11
H29	VSS	AL13
H3	VSS	AL17
H35	VSS	AL19
J10	VSS	AL24
J11	VSS	AL29
J3	VSS	AL32
J35	VSS	AL33
J38	VSS	AL38
J5	VSS	AM15
T42	VSS	AM17
U10	VSS	AM19
U11	VSS	AM22
U14	VSS	AM24
U17	VSS	AM27
U18	VSS	AM29
U28	VSS	AM45
U29	VSS	AN11
U31	VSS	AN22
U32	VSS	AN27
U33	VSS	AN31
U38	VSS	AN39
U4	VSS	AN7
U8	VSS	AN8
V18	VSS	AP11
V20	VSS	AP4
V21	VSS	AR33
V23	VSS	AR34
V25	VSS	AR42
V29	VSS	AR9
V3	VSS	AT10
V45	VSS	AT15
W14	VSS	AT36
W31	VSS	AT8
W32	VSS	AU1
W33	VSS	AU35
W38	VSS	AU36
W4	VSS	AU39
W8	VSS	AU45
Y17	VSS	C4
	VSS	

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SKL-H-PCH\_BGA837

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		B		1.0	
		Document Number		Date	
		LA-E152P		Thursday, November 10, 2016	
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Priority : AR -> WIGI/VGA(PS8338)

AR

WIGI/VGA(PS8338)



Port switching control or prioritP configuration. Internal pull down -150KΩ, 3.3V I/O  
For Control Switching Mode (CFG0 = L):  
SW = L: Port1 is selected (default)  
SW = H: Port2 is selected  
For Automatic Switching Mode (CFG0 = H):  
SW = L: Port1 has higher prioritP when both ports are plugged (default)  
SW = H: Port2 has higher prioritP when both ports are plugged

vender suggest MUX use LLEQ, PEQ=M and PIO=H !!

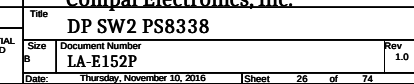
Programmable input equalization levels, Internal pull down at -150Kohm, 3.3V I/O  
PEQ =  
L: default, LEQ, compensate channel loss up to 11.5dB @HBR2  
H: HEQ, compensate channel loss up to 14.5dB @HBR2  
M: LLEQ, compensate channel loss up to 8.5dB @HBR2

PIO: Automatic EQ disable, Internal pull down -150K ohm, 3.3V I/O  
PIO = L: Automatic EQ enable (default)  
PIO = H: Automatic EQ disable

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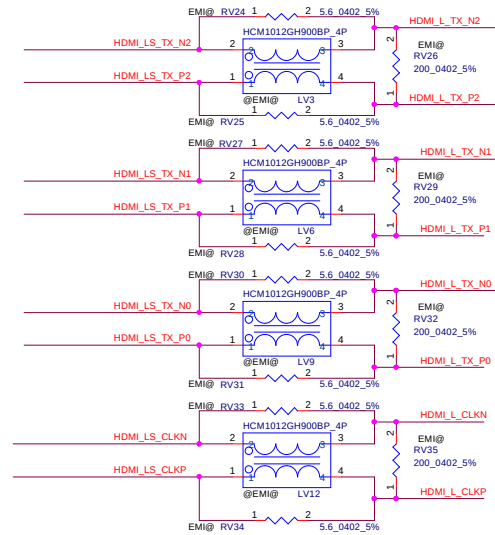
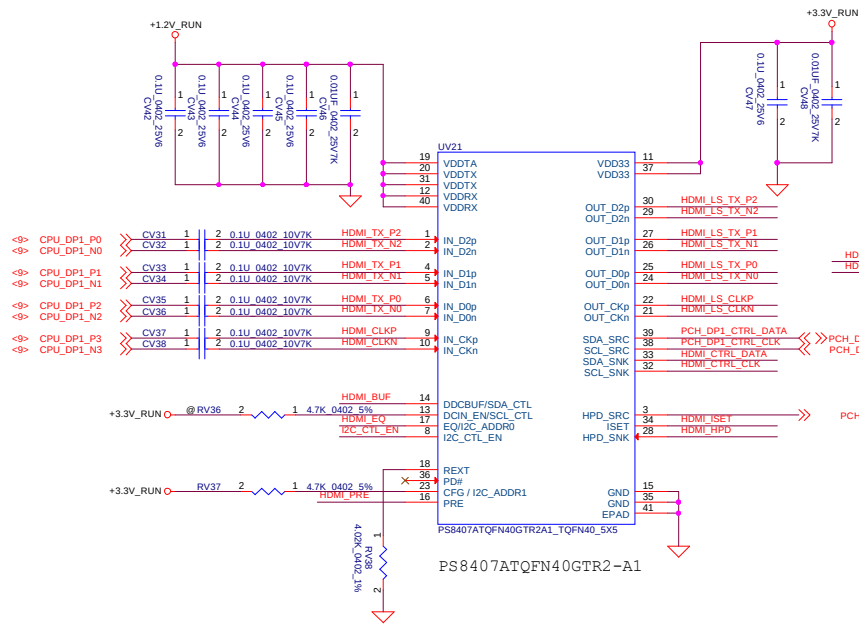
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title	DP SW1 PS8338		
Size	Document Number	Rev	
B	LA-E152P	1.0	
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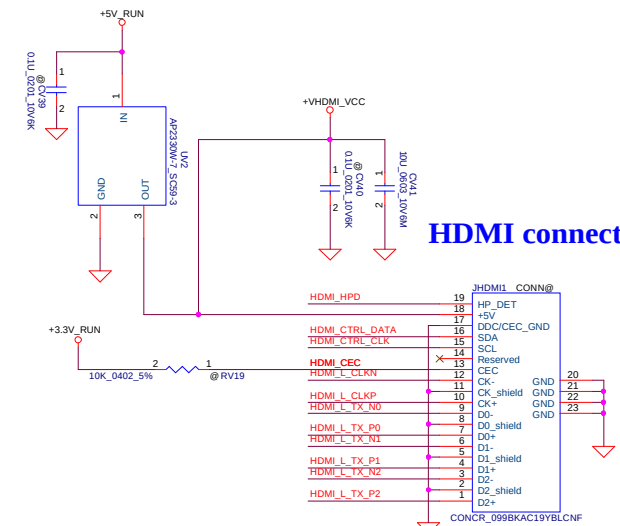




# For Breckenridge 15



## HDMI connector



Enable active DDC buffer: Internal pull down at ~150KΩ, 3.3V I/O.  
L: passive DDC pass-through(default)  
H: active DDC buffer with default threshold  
M: active DDC buffer without internal pull up resistor

Receiver equalization setting: Internal pull down at ~150KΩ, 3.3V I/O.  
L: programmable EQ for channel loss up to 12.4dB(default)  
H: programmable EQ for channel loss up to 4.3dB  
M: programmable EQ for channel loss up to 8.6dB

I2C Control enable: Internal pull down at 150KΩ, 3.3V I/O.  
L: Pin control is selected with auto jitter cleaning(default)  
H: I2C control is selected with default I2C address  
M: Pin control is selected with full jitter cleaning

TMDs output swing adjustment: Internal pull down at ~150KΩ, 3.3V I/O.  
L: default, 1000mV  
H: increase +13%  
M: reduce -13%

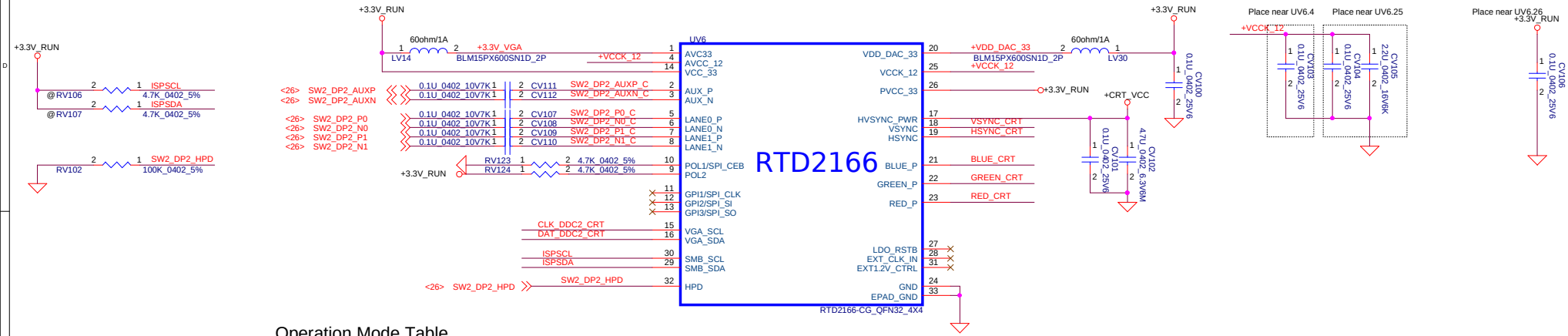
Output pre-emphasis setting: Internal pull down at ~150KΩ, 3.3V I/O.  
L: no pre-emphasis(default)  
H: 1.6dB pre-emphasis  
M: 2.5dB pre-emphasis

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HDMI CONN			
Size B	Document Number LA-E152P	Rev 1.0	
Date: Thursday, November 10, 2016	Sheet 27	of 74	



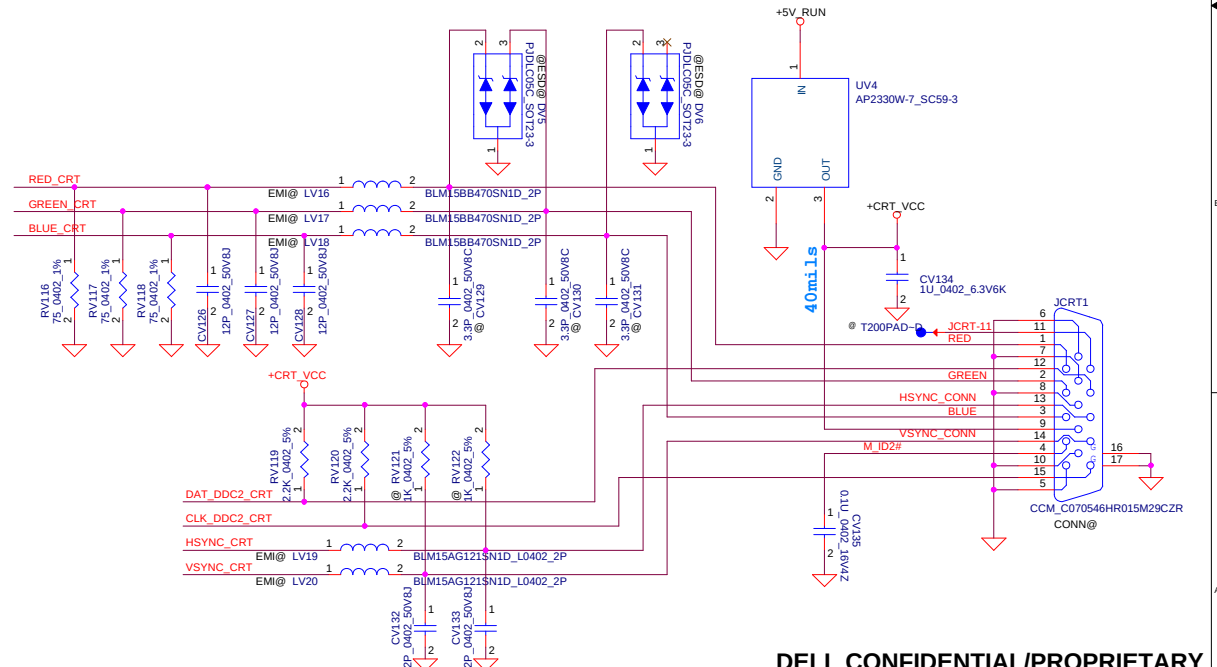
For TBT SW2\_DP2  
For non-TBT SW1\_DP2

For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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Compal Electronics, Inc.

DP to VGA & VGA Conn



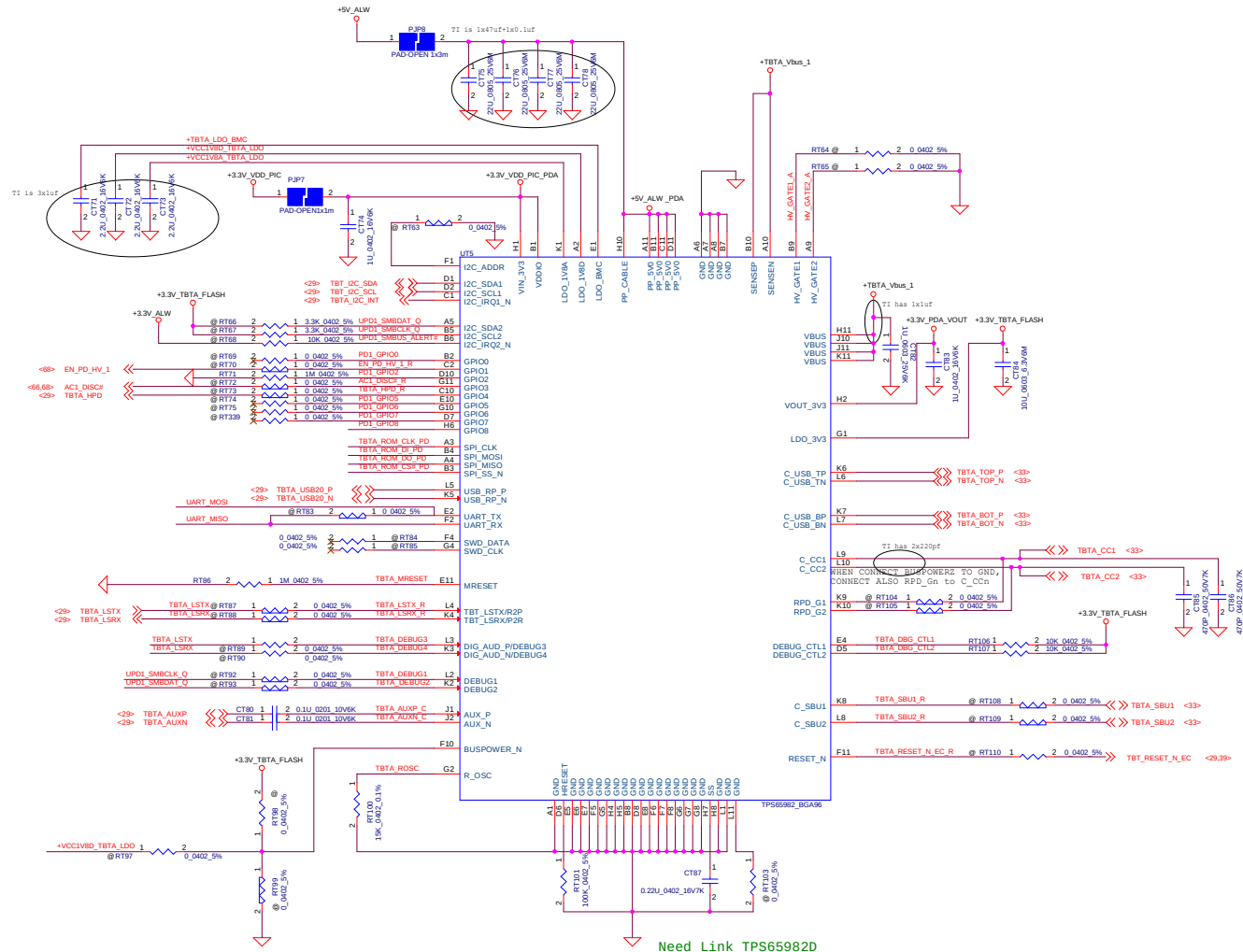
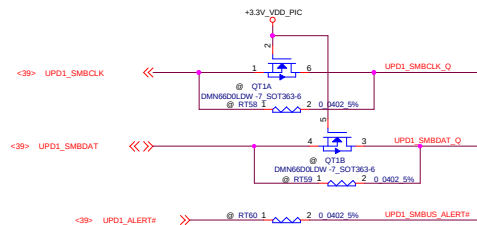
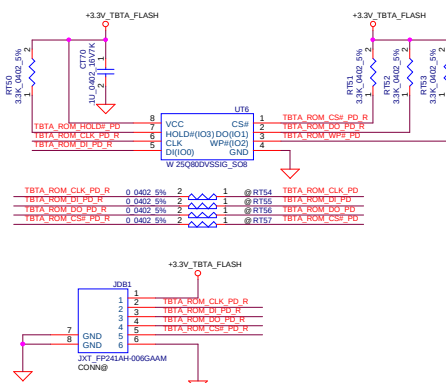








For AR Config



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFF only SV (0/0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TV VID supported
0.10	0.18	1	UFF only SV (0/0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes - Sink, C and D pin configuration TV VID supported
0.20	0.28	2	UFF only SV (0/0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TV VID supported
0.30	0.38	3	UFF only SV (0/3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Sink, C and D pin configuration TV VID supported
0.40	0.48	4	DPR SV (0/0.9-3.0A Sink capability SV (3/3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TV VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DPR SV (0/0.9-3.0A Sink capability SV (3/3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TV VID supported Accepts power role swaps but will not initiate. Accepts data role swaps in UFP and can initiate.
0.60	0.68	6	DPR SV (0/0.9-3.0A Sink capability SV (3/3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TV VID supported Accepts power role swaps but will not initiate. Accepts data role swaps in DPR and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

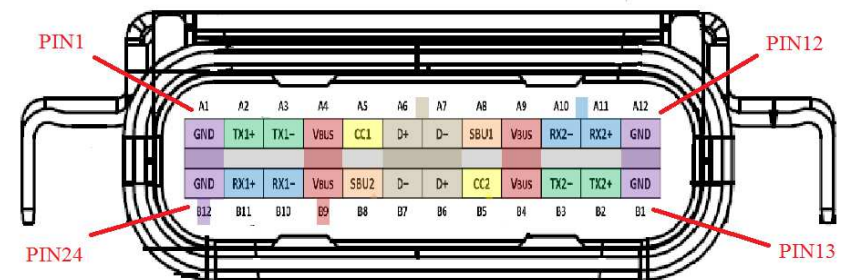
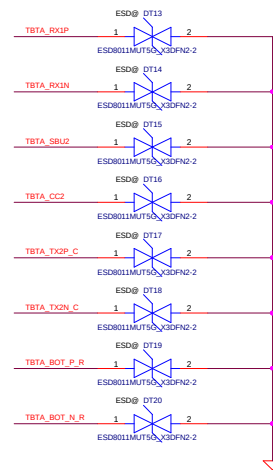
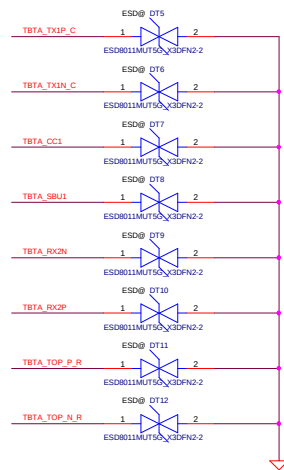
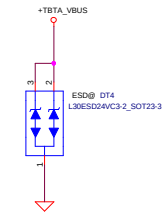
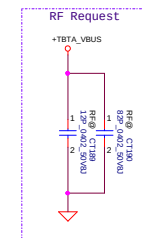
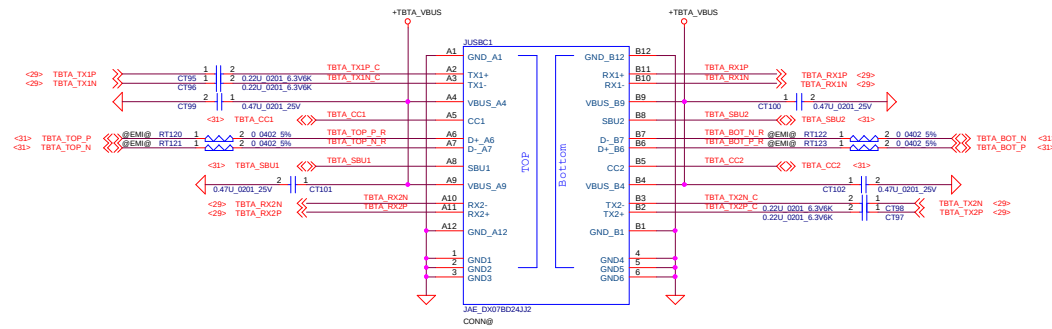
Need Link TPS65982D







For AR Config



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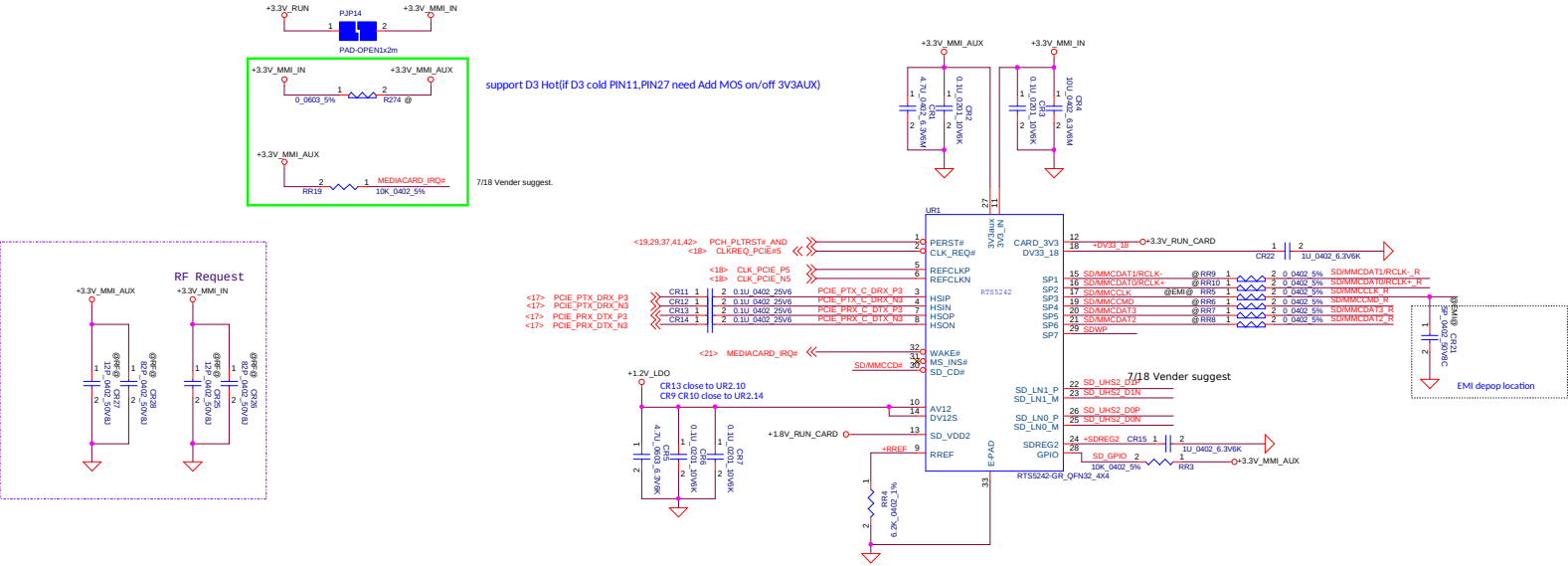




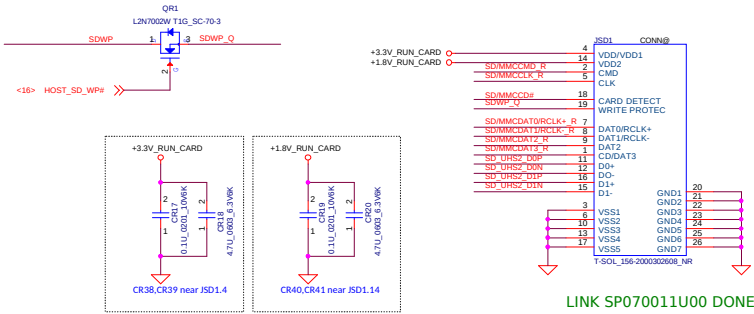




For PCIE Interface

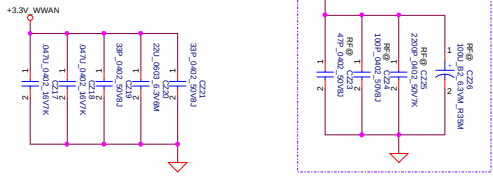
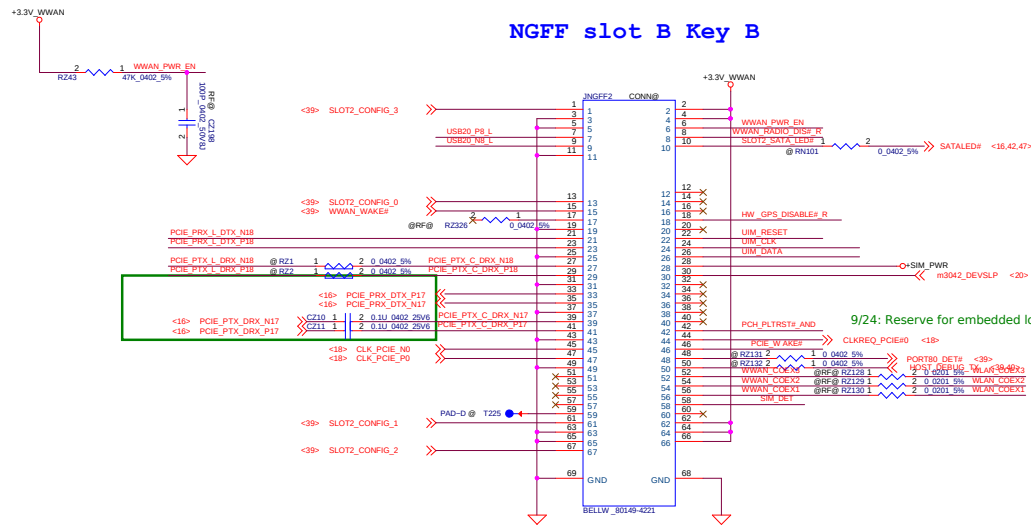


HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



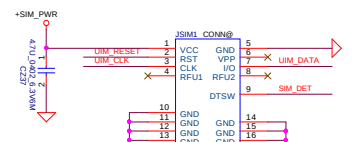


## NGFF slot B Key B

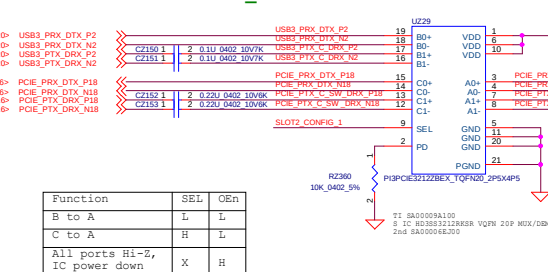


STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

## SIM Card Push-Push



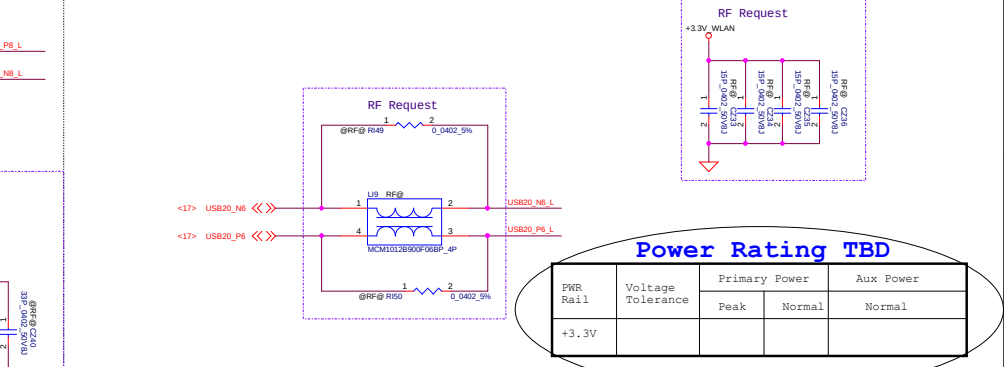
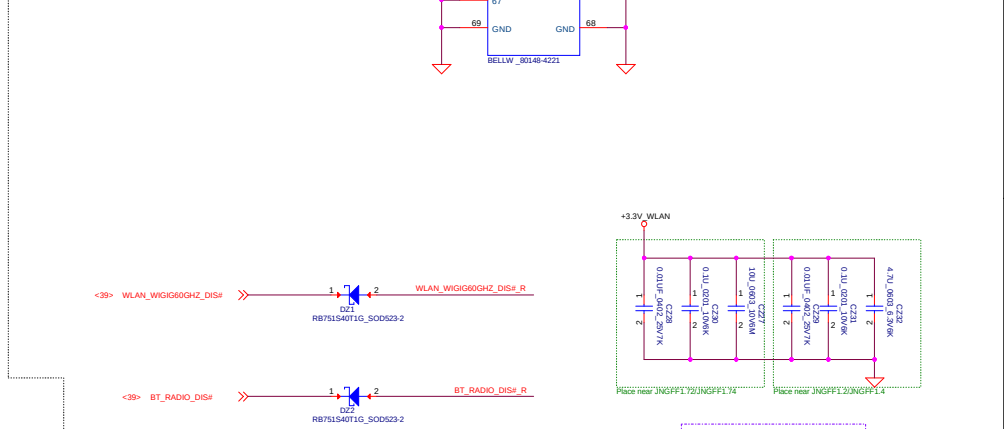
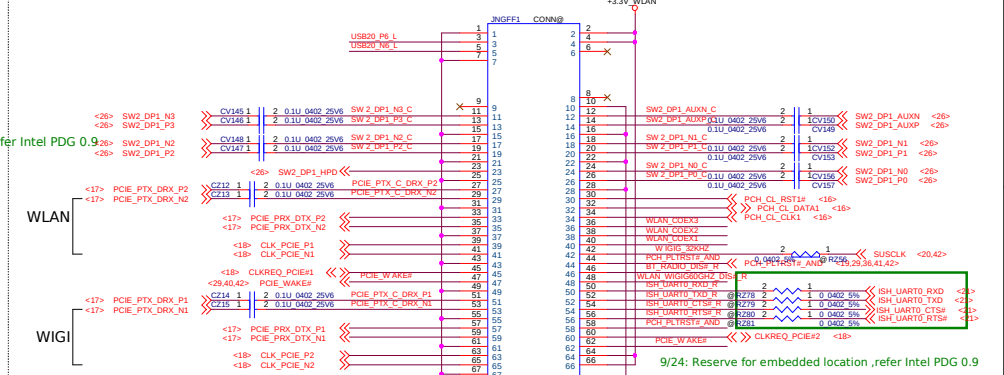
## T-SQ\_5-991503004000-6 LINK DONE



## for Breckenridge 15 DSC

For TBT SW2\_DP1  
For non-TBT SW1\_DP1

## NGFF slot A Key A 80148-3221680148-4221 Footprint the same



## Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power	Aux Power
+3.3V		Peak	Normal

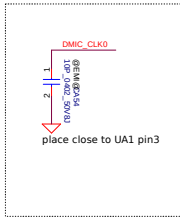
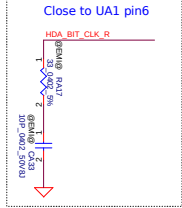
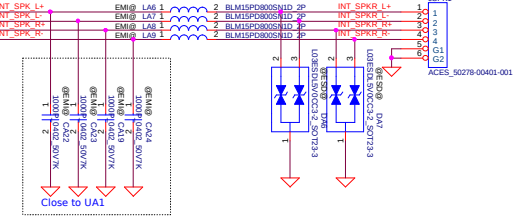
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Title		Document Number	
NGFF Card		LA-E152P	
Date	Thursday, November 10, 2016	Sheet	37 of 74



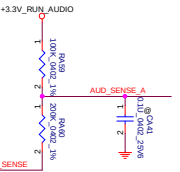
1W x 1ch, 40mm (Transducer spec is 80mW/0.5Watt per unit, there are two transducer units in one speaker box.)

## Internal Speakers Header

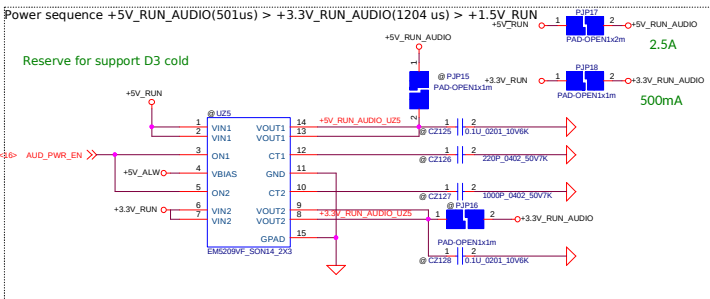
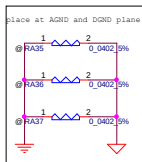
40 mils trace keep 20 mil spacing



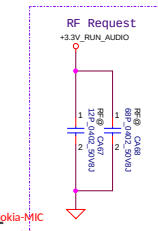
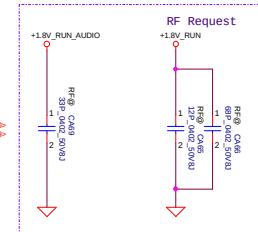
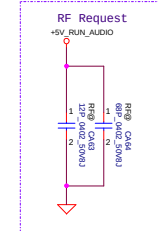
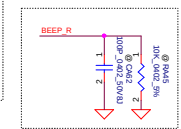
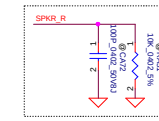
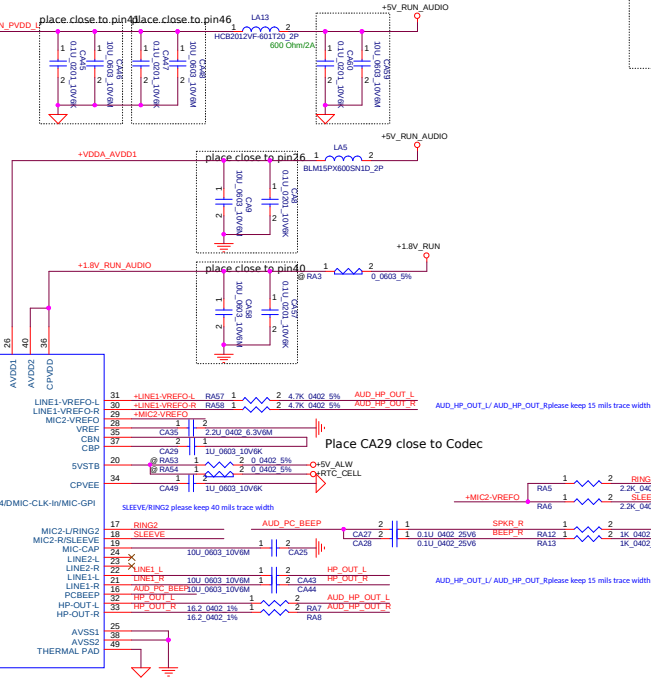
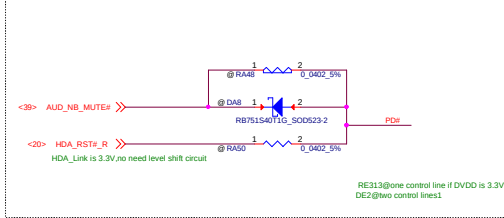
Place closely to Pin 13.



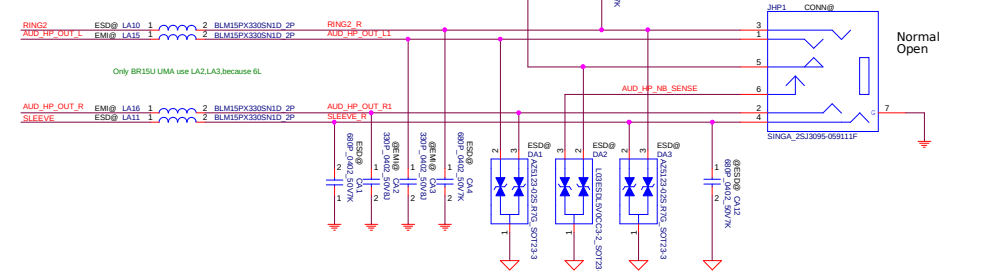
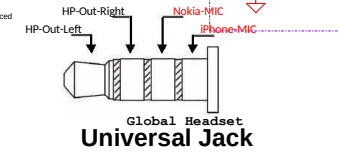
Add for solve pop noise and detect issue



## CLASS-D POWER DOWN CONTROL CIRCUIT

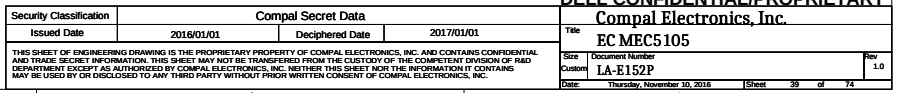


Add this Filter to avoid other components/chips are influenced

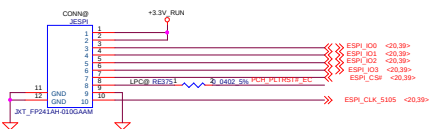
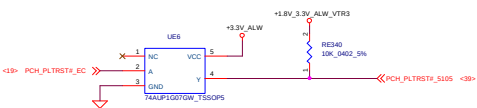


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Size	Document Number	Rev	1.0
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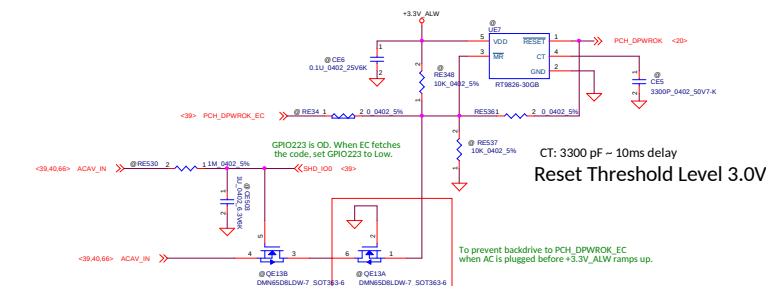






LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

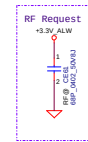
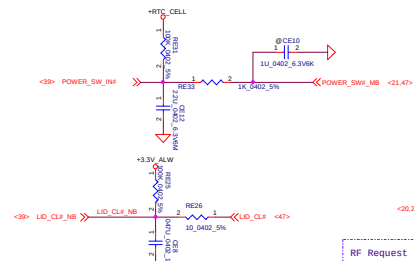
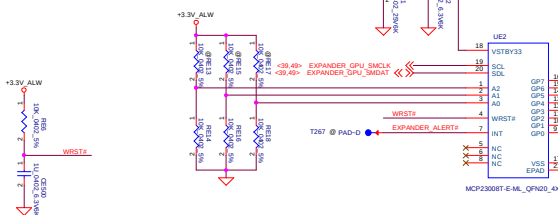
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



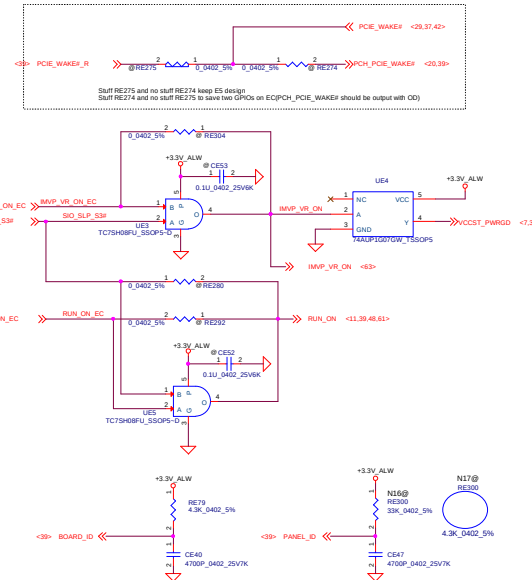
In DC mode, ACAP\_IN is LOW. This circuit doesn't affect PCH\_DPWRK#.  
In AC mode, 1. ACAP\_IN is high. GPIO223 is tri-state. QE138 is ON. QE13A can prevent backdrive to PCH\_DPWRK#.  
2. EC fetches code and drives GPIO223 to LOW to turn off QE138. When QE138 is off, un-plug/plug AC will not affect DSW\_DPWRK#.  
3. When WD7 occurs, GPIO223 is tri-state (EC reset). ACAP\_IN charges CE503. When AC is removed, ACAP\_IN goes LOW immediately.  
QE138 still keeps on according to RC discharging rate. PCH\_DPWRK# is LOW because ACAP\_IN is LOW.

Control Byte	S	1	0	0	0	A2	A1	A0	R/W
R/W = 0 = Write R/W = 1 = Read									

SMBus address 0x40



RE343	CE62	REV
240K 4700p		Single Port ACE w/o AR
130K 4700p		Single Port ACE w/AR
62K 4700p		Dual Port ACE w/o AR
33K 4700p		Dual Port ACE w/AR
8.2K 4700p		Dual Port ACE (w/AR +w/o AR)
4.3K 4700p		
2K 4700p		
1K 4700p		



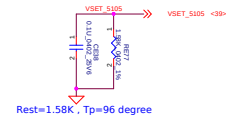
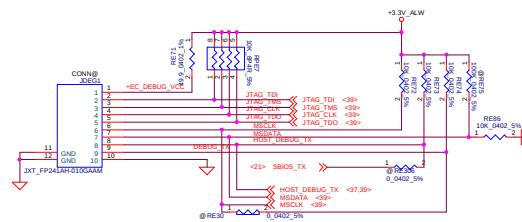
RE79	CE40	REV
240K 4700p		X00
130K 4700p		X01
62K 4700p		X02
33K 4700p		X03
8.2K 4700p		
4.3K 4700p		A00
2K 4700p		
1K 4700p		

RE300	CE47	PANEL SIZE
240K 4700p		12"
130K 4700p		14"
33K 4700p		BR15 H
4.3K 4700p		BR15 P

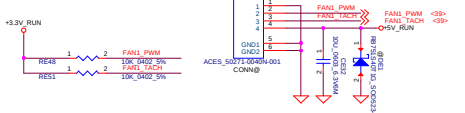
PD\_ACE\_De# rise time is measured from 5%~68%

BOARD\_ID rise time is measured from 5%~68%

PANEL\_ID rise time is measured from 5%~68%



Link 50271-0040N-001 DONE



Thermal diode mapping

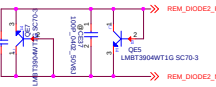
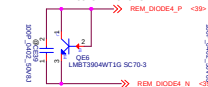
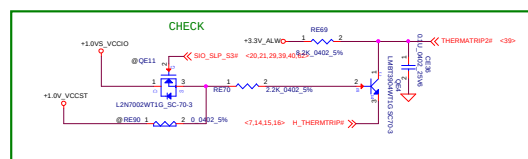
5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU  
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to Type-C and CE37 close to QE5

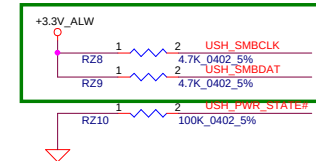
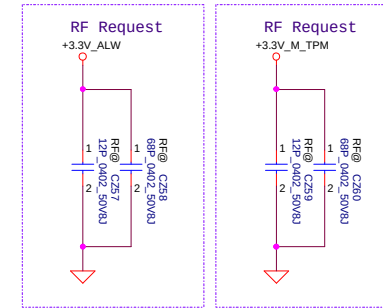
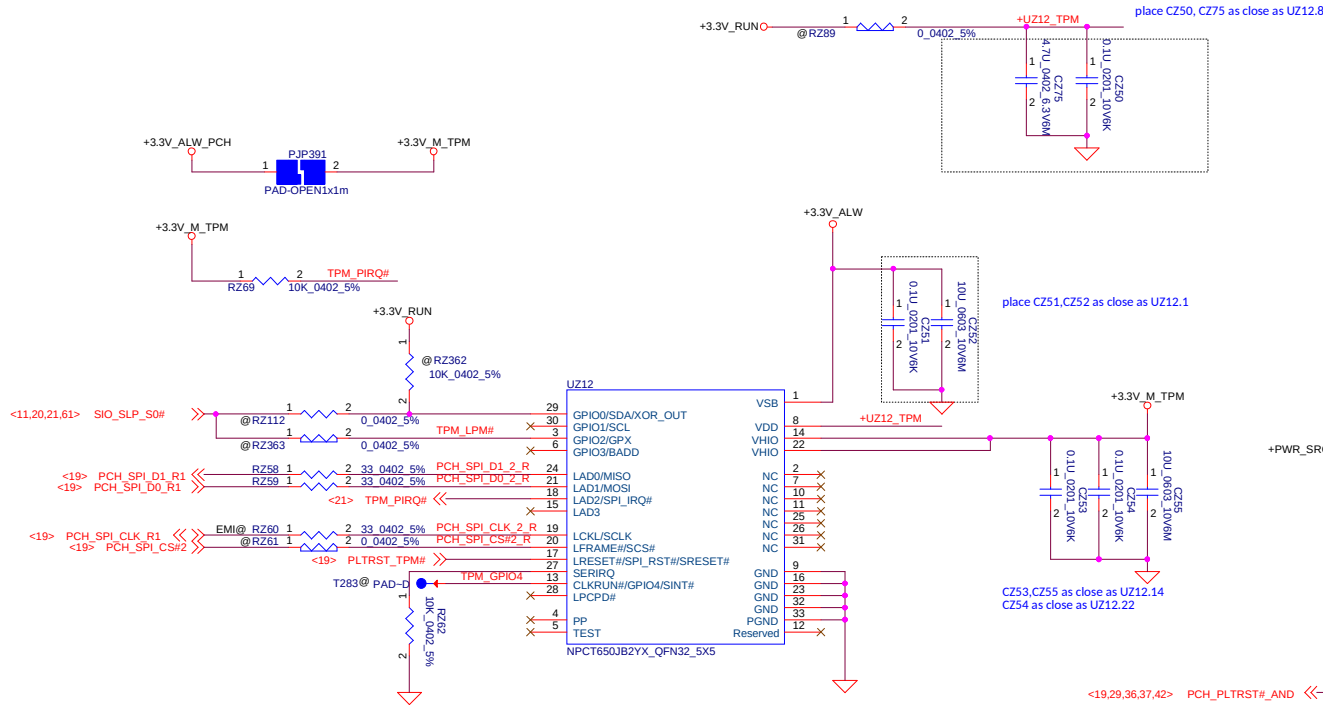
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR Choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

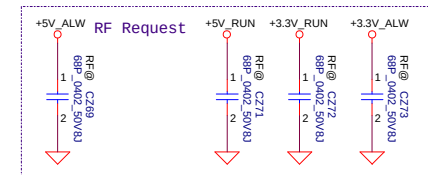
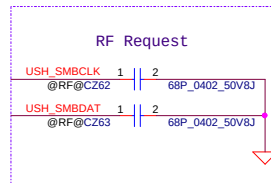
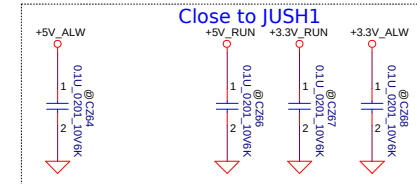
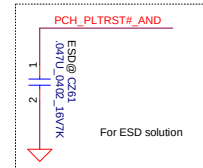
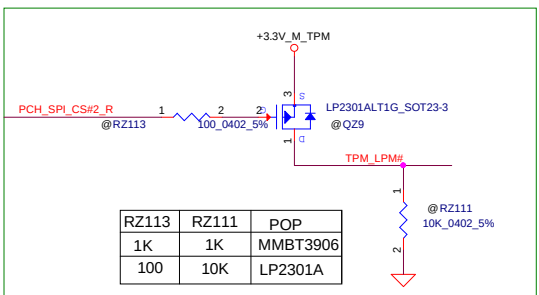
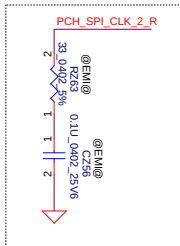
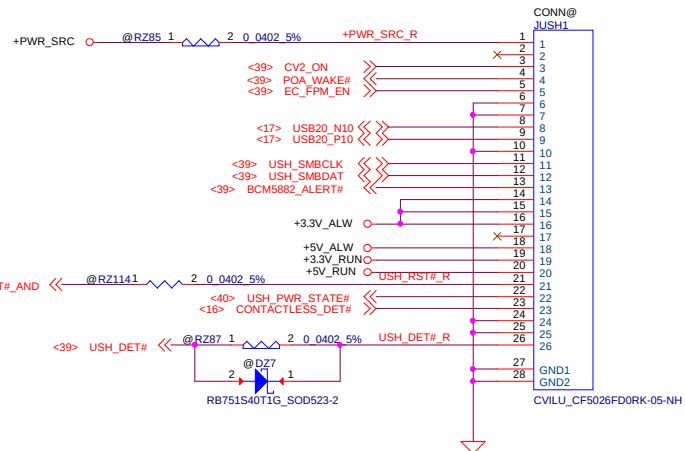




# For NUVOTON TPM



## USH CONN




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RF Request

+3.3V\_HDD\_M2

1

2

@RF@CH60  
68P 0u02 50V/8J



+3.3V RUN

SATALED# &lt;16,37,47&gt;

<20>

AND <19,29,36,37,41>  
3 <18>

<29,37,40>

◀ SUSCLK <20,37>

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2017/01/01

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COMPETENT DIVISION OF THE FBI.

INFORMATION IT CONTAINS  
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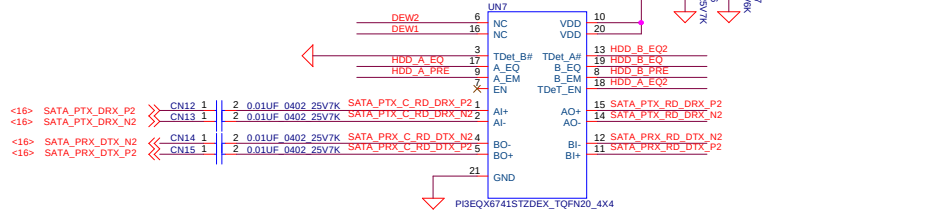
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

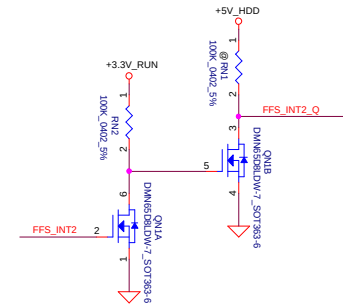
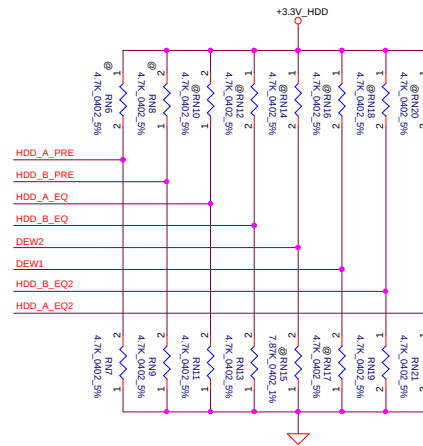
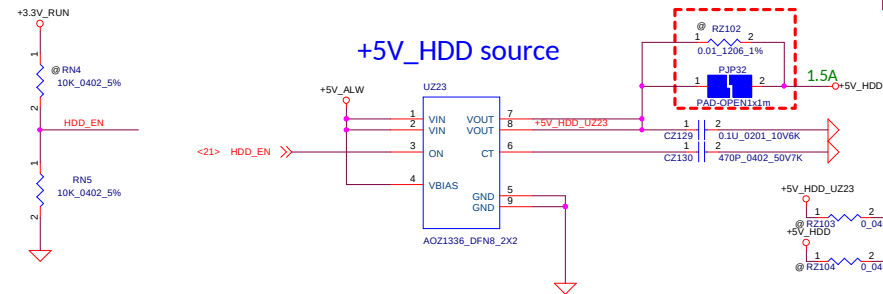
## SATA Repeater



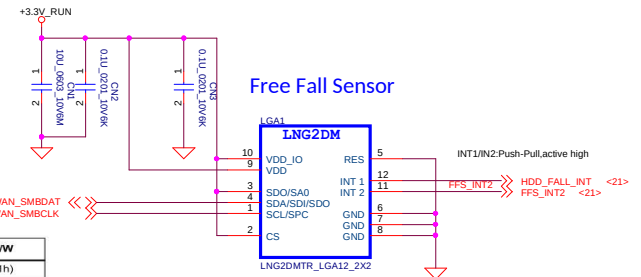
	HDD_A_EQ2 PIN17	HDD_B_EQ2 PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	NC (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		1	6dB	6dB	NC		
		1	9dB	9dB	1.5dB	1.5dB	
2nd	TI	0	7dB	7dB	0	0dB	0dB
		1	9dB	9dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB			
		M M	12.2dB	12.2dB	0 M	0dB	0dB
		M 0	9.4dB	9.4dB	1	-3.5dB	-3.5dB
		M 1	13.3dB	13.3dB		-6dB	-6dB
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

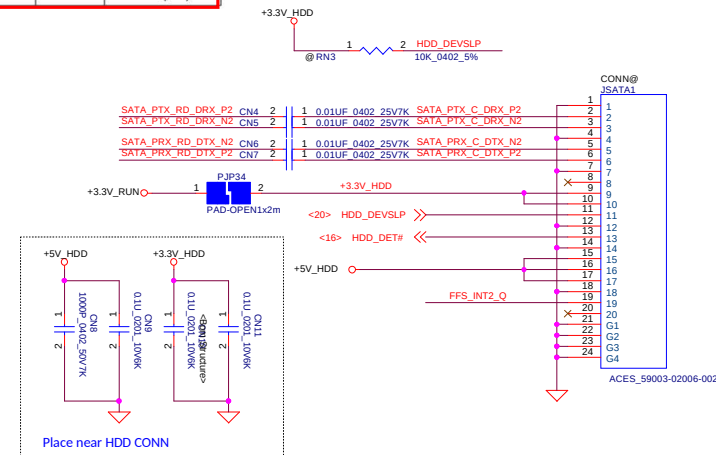
\*red color is current setting



## Free Fall Sensor



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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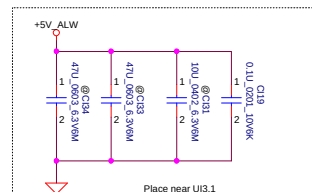
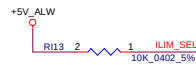
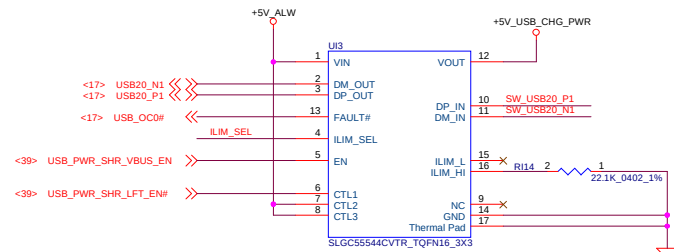
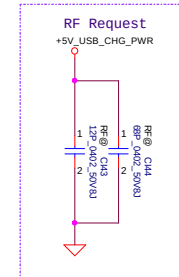
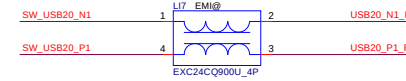
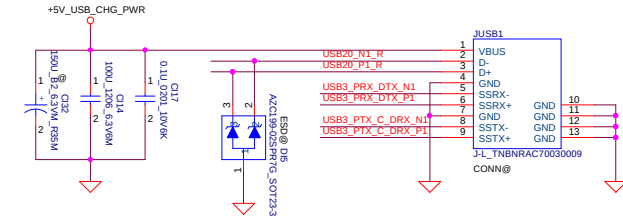
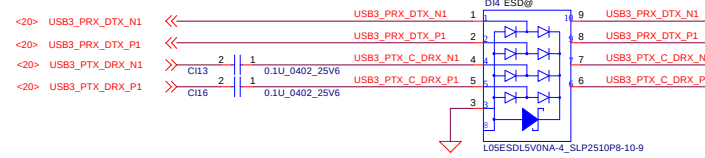
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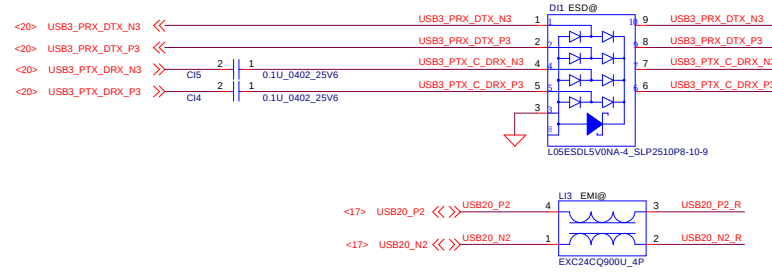
# For PWR SW + Charger combine IC



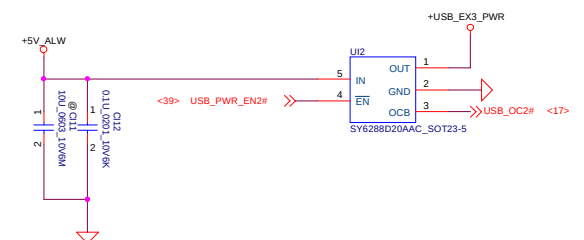
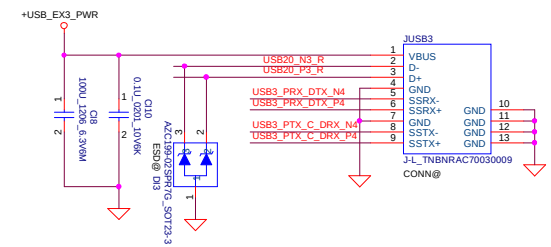
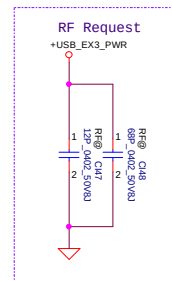
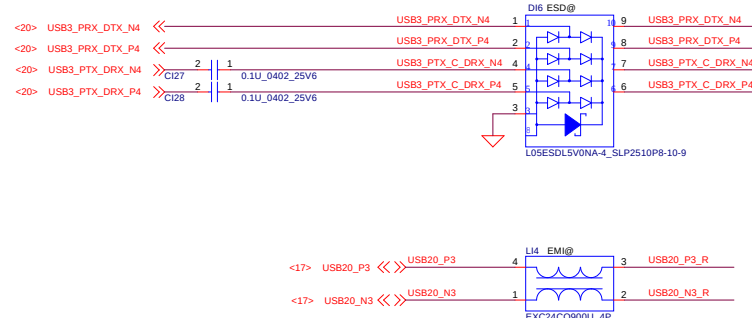
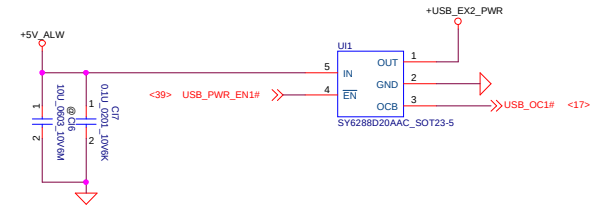
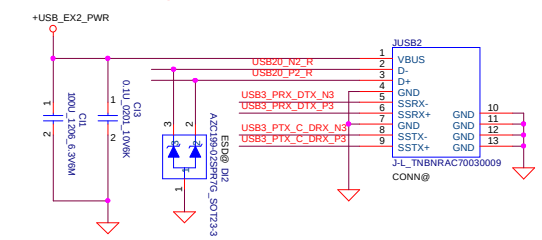
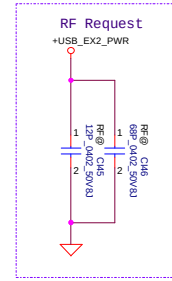
Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc.					
Issued Date	2016/01/01	Deciphered Date	2017/01/01	Title	USB SW				
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					LA-E152P	1.0			
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# For Breckenridge 14&15/Steamboat 14



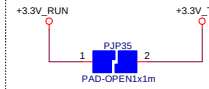
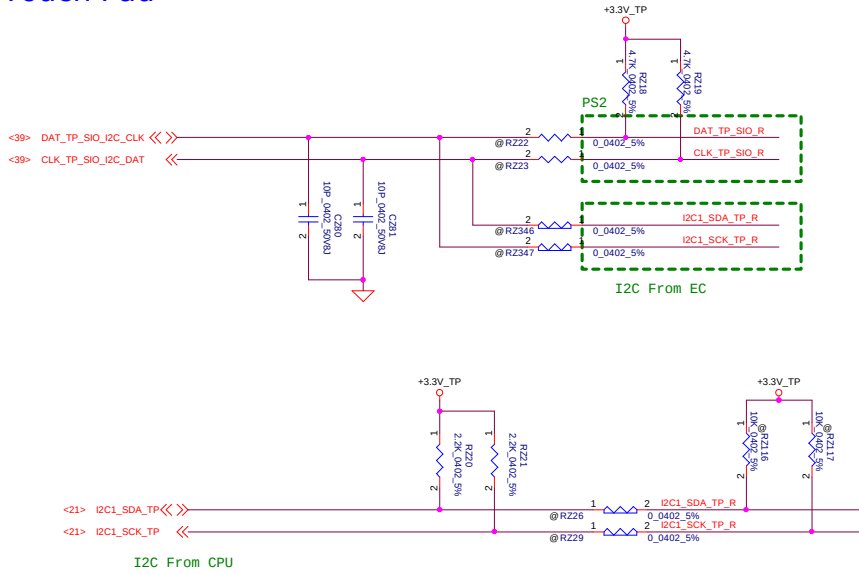
DfB request:  
main SM070003200 (NPAQ\_MCM1012B900F06BP\_4P)  
Footprint use 2nd source SM070004400 (PANAS\_EXC24CQ900U\_4P)  
Pitch change from 0.5mm to 0.55mm



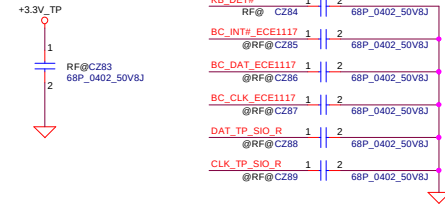
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				Deciphered Date				Compal Electronics, Inc.			
2016/01/01				2017/01/01				JUSB2&JUSB3			
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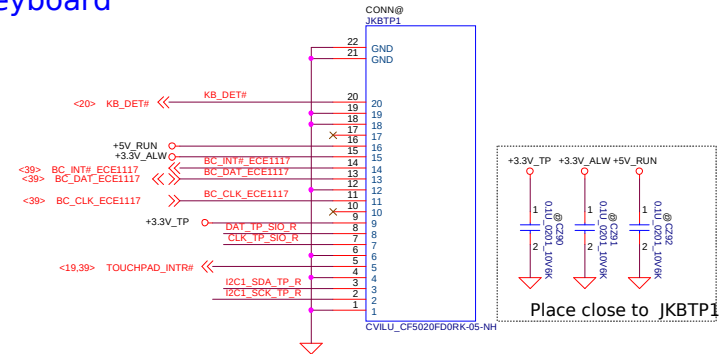
## Touch Pad



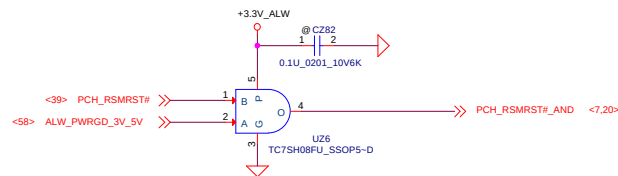
## RF Request



## Keyboard



## RSMRST circuit

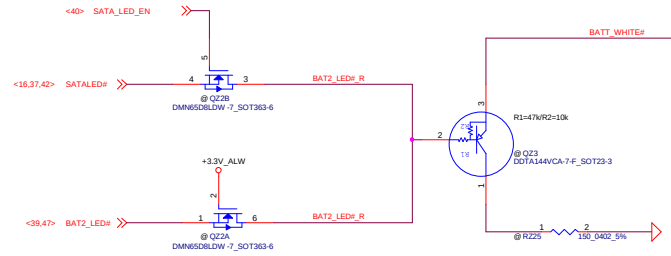


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2016/01/01		2017/01/01		Title	
				Keyboard	
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## HDD LED MUX

means E/C can switch battery white led and HDD LED by hot key "Fn+H"

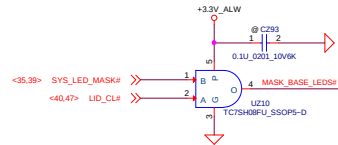
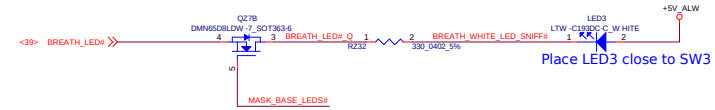


## Battery LED

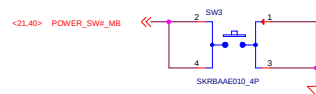


## Breath LED

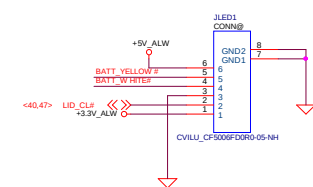
LED PIN change to SC50000FL00 from SC50000BA00



## POWER & INSTANT ON SWITCH



## LED board CONN

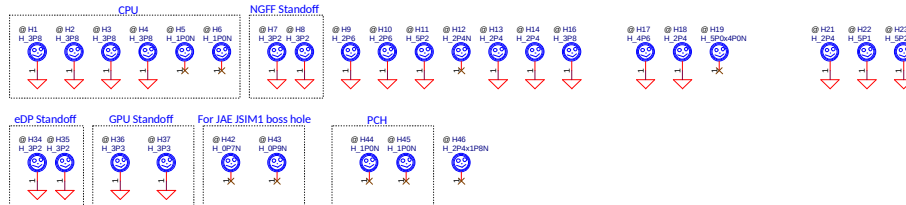


### Fiducial Mark



### LED Circuit Control Table

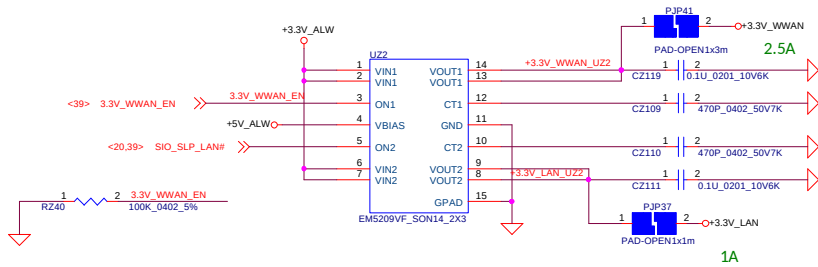
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



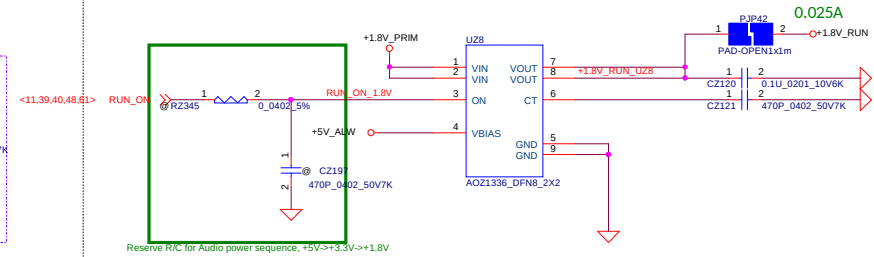
Security Classification			Compal Secret Data		Title	
Issued Date			2016/01/01	Deciphered Date	2017/01/01	Document Number
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Date			Thursday, November 10, 2016	Sheet	47 of 74	



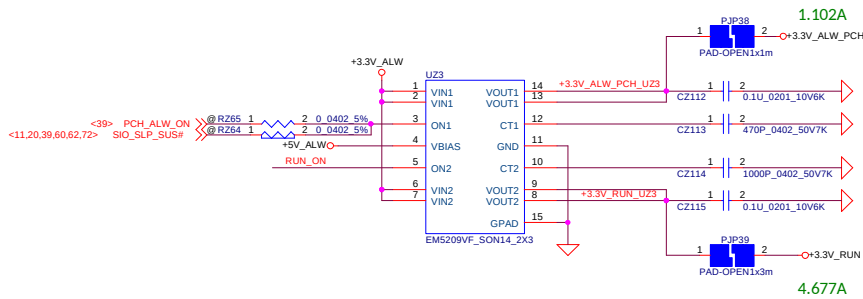
### +3.3V\_WWAN/+3.3V\_LAN source



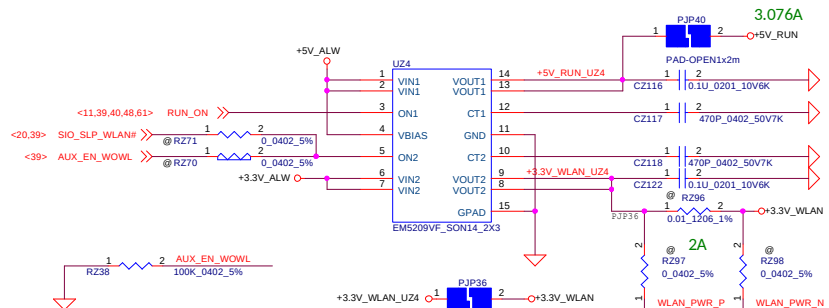
### +1.8V\_RUN source



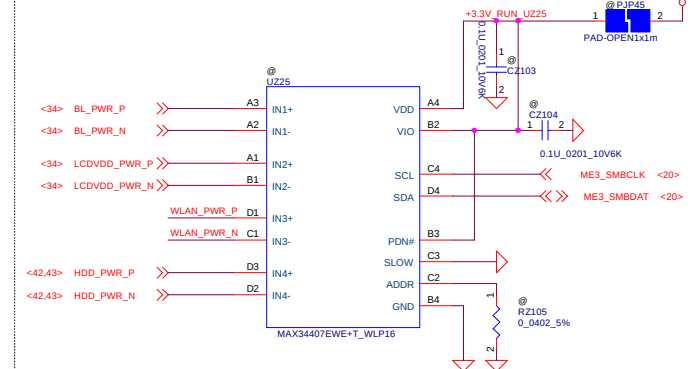
### +3.3V\_ALW\_PCH/+3.3V\_RUN source



### +5V\_RUN/+3.3V\_WLAN source



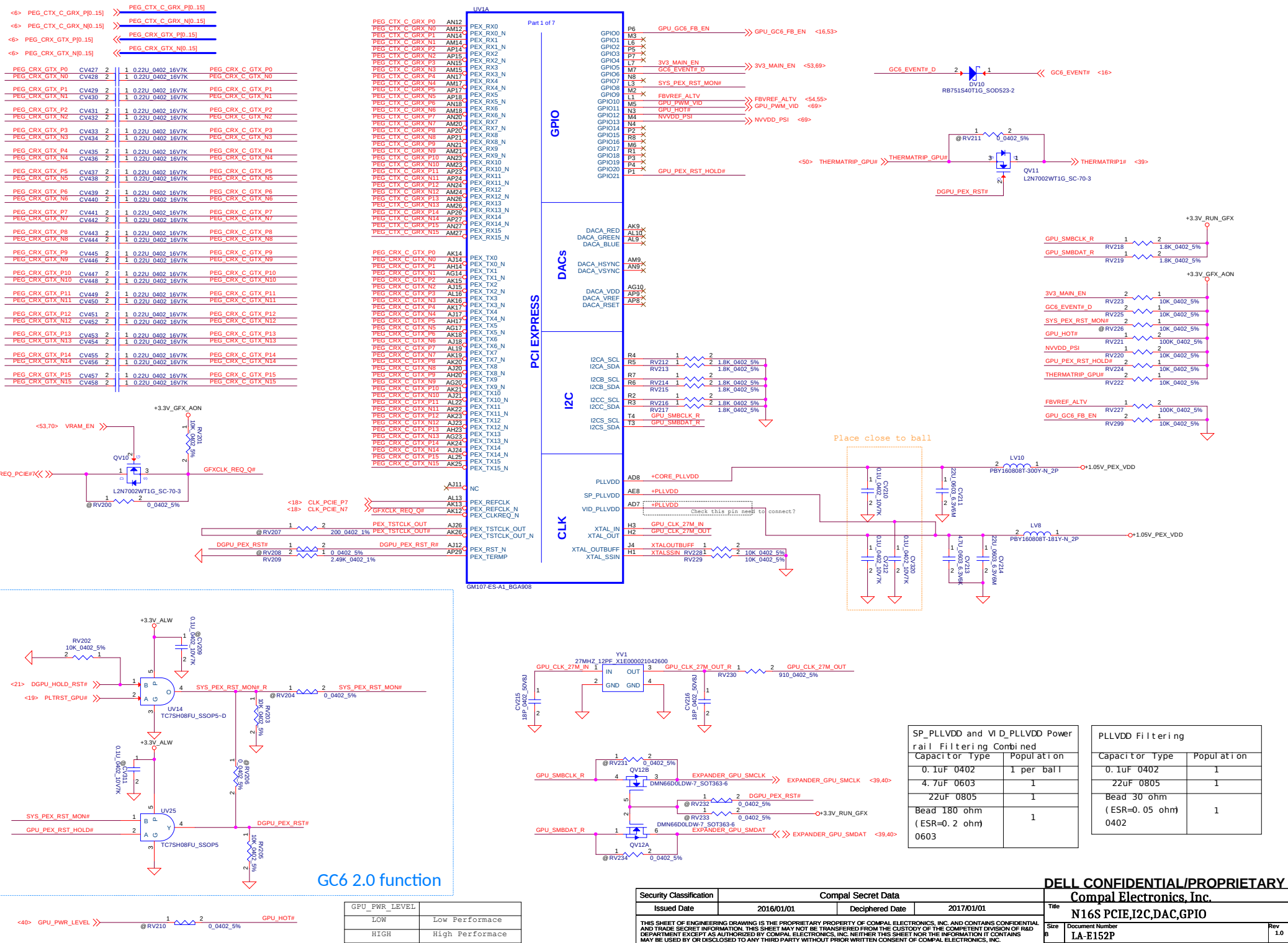
### BR15H Only



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Security Classification	Compal Secret Data		Title	
Issued Date	2016/01/01	Deciphered Date	2017/01/01	Power control
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GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace

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<b>DELL CONFIDENTIAL/PROPRIETARY</b>			
<b>Compal Electronics, Inc.</b>			
Title <b>N16S PCIE,I2C,DAC,GPIO</b>			
Size B	Document Number <b>LA-E152P</b>		Rev <b>1.0</b>



SMBUS_ALT_ADDR	Description
0	0x9E( Default )
1	0x9C( Multi - GPU usage)

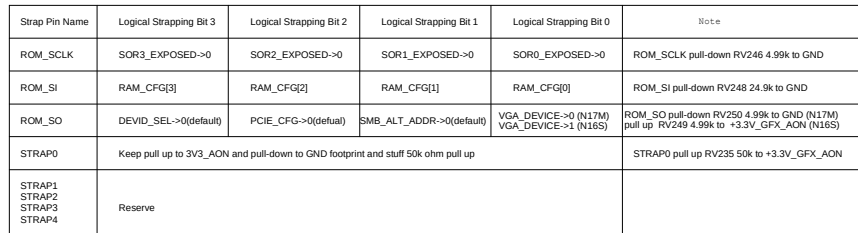
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

Resistor Value	Pull-up to VDD3	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
4 Gb	128Nx32	1.35V	Samsung	K4G4132SF-HC28	E-die	0x7	5 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BAG-60-F	A-die	0x4	5 Gbps	N/A	Full	Production candidate

The schematic diagram illustrates the power plane for the NVIDIA Jetson Nano module, showing the distribution of 3.3V\_GFX\_AON and 3.3V\_RUN\_GFX supplies. The components are labeled as follows:

- 3.3V\_GFX\_AON Supply:**
  - Resistors: R1023 (40.9K, 0.002, 1%), R1024 (40.9K, 0.002, 1%), R1025 (40.9K, 0.002, 1%), R1026 (2K, 0.002, 1%), R1027 (2K, 0.002, 1%), R1028 (2K, 0.002, 1%), R1029 (2K, 0.002, 1%), R1030 (2K, 0.002, 1%), R1031 (2K, 0.002, 1%), R1032 (2K, 0.002, 1%), R1033 (2K, 0.002, 1%), R1034 (2K, 0.002, 1%), R1035 (2K, 0.002, 1%), R1036 (2K, 0.002, 1%), R1037 (2K, 0.002, 1%), R1038 (2K, 0.002, 1%), R1039 (2K, 0.002, 1%), R1040 (2K, 0.002, 1%), R1041 (2K, 0.002, 1%), R1042 (2K, 0.002, 1%), R1043 (2K, 0.002, 1%), R1044 (2K, 0.002, 1%), R1045 (2K, 0.002, 1%), R1046 (2K, 0.002, 1%), R1047 (2K, 0.002, 1%), R1048 (2K, 0.002, 1%), R1049 (2K, 0.002, 1%), R1050 (2K, 0.002, 1%), R1051 (2K, 0.002, 1%), R1052 (2K, 0.002, 1%), R1053 (2K, 0.002, 1%), R1054 (2K, 0.002, 1%), R1055 (2K, 0.002, 1%), R1056 (2K, 0.002, 1%), R1057 (2K, 0.002, 1%), R1058 (2K, 0.002, 1%), R1059 (2K, 0.002, 1%), R1060 (2K, 0.002, 1%), R1061 (2K, 0.002, 1%), R1062 (2K, 0.002, 1%), R1063 (2K, 0.002, 1%), R1064 (2K, 0.002, 1%), R1065 (2K, 0.002, 1%), R1066 (2K, 0.002, 1%), R1067 (2K, 0.002, 1%), R1068 (2K, 0.002, 1%), R1069 (2K, 0.002, 1%), R1070 (2K, 0.002, 1%), R1071 (2K, 0.002, 1%), R1072 (2K, 0.002, 1%), R1073 (2K, 0.002, 1%), R1074 (2K, 0.002, 1%), R1075 (2K, 0.002, 1%), R1076 (2K, 0.002, 1%), R1077 (2K, 0.002, 1%), R1078 (2K, 0.002, 1%), R1079 (2K, 0.002, 1%), R1080 (2K, 0.002, 1%), R1081 (2K, 0.002, 1%), R1082 (2K, 0.002, 1%), R1083 (2K, 0.002, 1%), R1084 (2K, 0.002, 1%), R1085 (2K, 0.002, 1%), R1086 (2K, 0.002, 1%), R1087 (2K, 0.002, 1%), R1088 (2K, 0.002, 1%), R1089 (2K, 0.002, 1%), R1090 (2K, 0.002, 1%), R1091 (2K, 0.002, 1%), R1092 (2K, 0.002, 1%), R1093 (2K, 0.002, 1%), R1094 (2K, 0.002, 1%), R1095 (2K, 0.002, 1%), R1096 (2K, 0.002, 1%), R1097 (2K, 0.002, 1%), R1098 (2K, 0.002, 1%), R1099 (2K, 0.002, 1%), R1100 (2K, 0.002, 1%), R1101 (2K, 0.002, 1%), R1102 (2K, 0.002, 1%), R1103 (2K, 0.002, 1%), R1104 (2K, 0.002, 1%), R1105 (2K, 0.002, 1%), R1106 (2K, 0.002, 1%), R1107 (2K, 0.002, 1%), R1108 (2K, 0.002, 1%), R1109 (2K, 0.002, 1%), R1110 (2K, 0.002, 1%), R1111 (2K, 0.002, 1%), R1112 (2K, 0.002, 1%), R1113 (2K, 0.002, 1%), R1114 (2K, 0.002, 1%), R1115 (2K, 0.002, 1%), R1116 (2K, 0.002, 1%), R1117 (2K, 0.002, 1%), R1118 (2K, 0.002, 1%), R1119 (2K, 0.002, 1%), R1120 (2K, 0.002, 1%), R1121 (2K, 0.002, 1%), R1122 (2K, 0.002, 1%), R1123 (2K, 0.002, 1%), R1124 (2K, 0.002, 1%), R1125 (2K, 0.002, 1%), R1126 (2K, 0.002, 1%), R1127 (2K, 0.002, 1%), R1128 (2K, 0.002, 1%), R1129 (2K, 0.002, 1%), R1130 (2K, 0.002, 1%), R1131 (2K, 0.002, 1%), R1132 (2K, 0.002, 1%), R1133 (2K, 0.002, 1%), R1134 (2K, 0.002, 1%), R1135 (2K, 0.002, 1%), R1136 (2K, 0.002, 1%), R1137 (2K, 0.002, 1%), R1138 (2K, 0.002, 1%), R1139 (2K, 0.002, 1%), R1140 (2K, 0.002, 1%), R1141 (2K, 0.002, 1%), R1142 (2K, 0.002, 1%), R1143 (2K, 0.002, 1%), R1144 (2K, 0.002, 1%), R1145 (2K, 0.002, 1%), R1146 (2K, 0.002, 1%), R1147 (2K, 0.002, 1%), R1148 (2K, 0.002, 1%), R1149 (2K, 0.002, 1%), R1150 (2K, 0.002, 1%), R1151 (2K, 0.002, 1%), R1152 (2K, 0.002, 1%), R1153 (2K, 0.002, 1%), R1154 (2K, 0.002, 1%), R1155 (2K, 0.002, 1%), R1156 (2K, 0.002, 1%), R1157 (2K, 0.002, 1%), R1158 (2K, 0.002, 1%), R1159 (2K, 0.002, 1%), R1160 (2K, 0.002, 1%), R1161 (2K, 0.002, 1%), R1162 (2K, 0.002, 1%), R1163 (2K, 0.002, 1%), R1164 (2K, 0.002, 1%), R1165 (2K, 0.002, 1%), R1166 (2K, 0.002, 1%), R1167 (2K, 0.002, 1%), R1168 (2K, 0.002, 1%), R1169 (2K, 0.002, 1%), R1170 (2K, 0.002, 1%), R1171 (2K, 0.002, 1%), R1172 (2K, 0.002, 1%), R1173 (2K, 0.002, 1%), R1174 (2K, 0.002, 1%), R1175 (2K, 0.002, 1%), R1176 (2K, 0.002, 1%), R1177 (2K, 0.002, 1%), R1178 (2K, 0.002, 1%), R1179 (2K, 0.002, 1%), R1180 (2K, 0.002, 1%), R1181 (2K, 0.002, 1%), R1182 (2K, 0.002, 1%), R1183 (2K, 0.002, 1%), R1184 (2K, 0.002, 1%), R1185 (2K, 0.002, 1%), R1186 (2K, 0.002, 1%), R1187 (2K, 0.002, 1%), R1188 (2K, 0.002, 1%), R1189 (2K, 0.002, 1%), R1190 (2K, 0.002, 1%), R1191 (2K, 0.002, 1%), R1192 (2K, 0.002, 1%), R1193 (2K, 0.002, 1%), R1194 (2K, 0.002, 1%), R1195 (2K, 0.002, 1%), R1196 (2K, 0.002, 1%), R1197 (2K, 0.002, 1%), R1198 (2K, 0.002, 1%), R1199 (2K, 0.002, 1%), R1200 (2K, 0.002, 1%), R1201 (2K, 0.002, 1%), R1202 (2K, 0.002, 1%), R1203 (2K, 0.002, 1%), R1204 (2K, 0.002, 1%), R1205 (2K, 0.002, 1%), R1206 (2K, 0.002, 1%), R1207 (2K, 0.002, 1%), R1208 (2K, 0.002, 1%), R1209 (2K, 0.002, 1%), R1210 (2K, 0.002, 1%), R1211 (2K, 0.002, 1%), R1212 (2K, 0.002, 1%), R1213 (2K, 0.002, 1%), R1214 (2K, 0.002, 1%), R1215 (2K, 0.002, 1%), R1216 (2K, 0.002, 1%), R1217 (2K, 0.002, 1%), R1218 (2K, 0.002, 1%), R1219 (2K, 0.002, 1%), R1220 (2K, 0.002, 1%), R1221 (2K, 0.002, 1%), R1222 (2K, 0.002, 1%), R1223 (2K, 0.002, 1%), R1224 (2K, 0.002, 1%), R1225 (2K, 0.002, 1%), R1226 (2K, 0.002, 1%), R1227 (2K, 0.002, 1%), R1228 (2K, 0.002, 1%), R1229 (2K, 0



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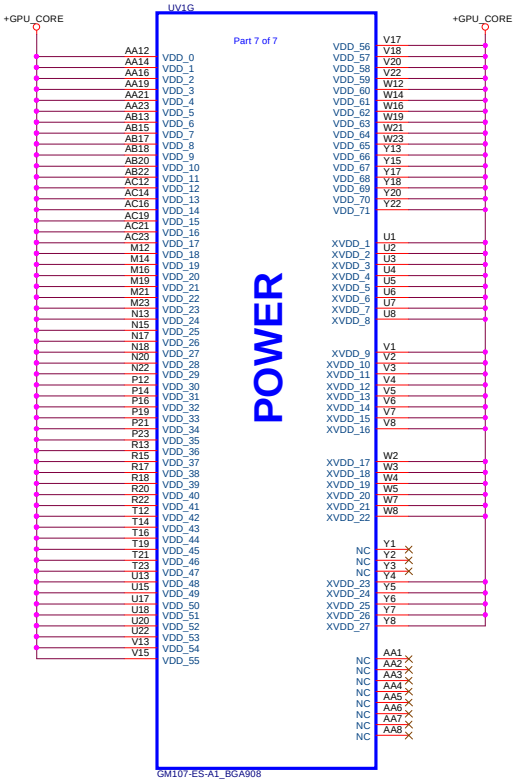
Size B	Document Number <b>LA-E152P</b>	Rev 1.0
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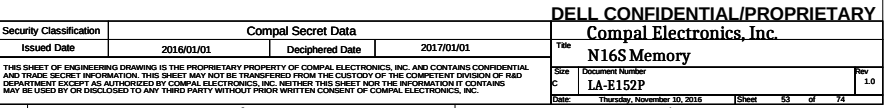


Caps on Power Side  
1UX8 4.7UX15 under GPU  
4.7UX5 22UX7 330UX1 near GPU



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								LA-E152P			
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								Sheet 52 of 74			
								Rev 1.0			





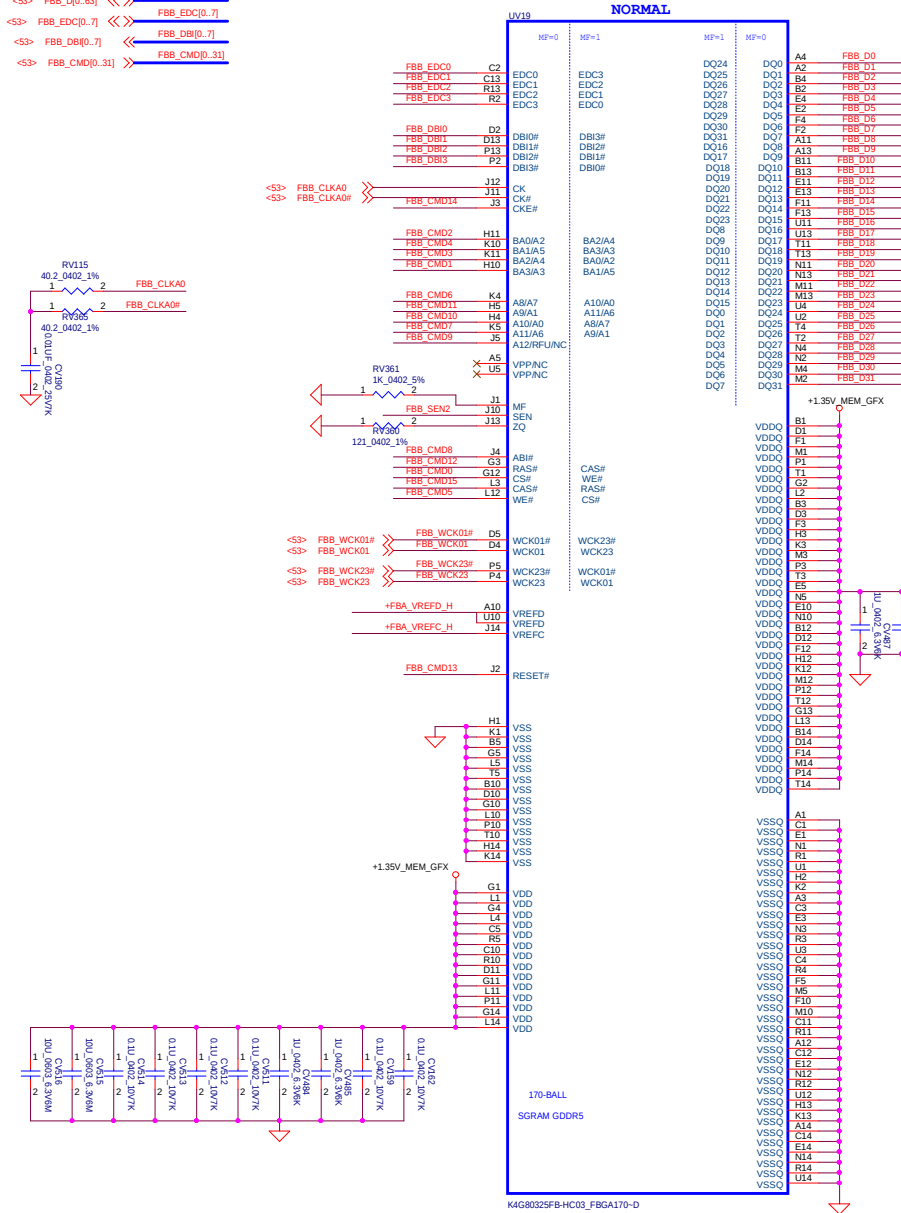




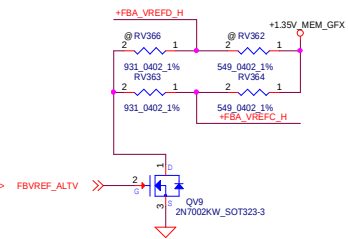
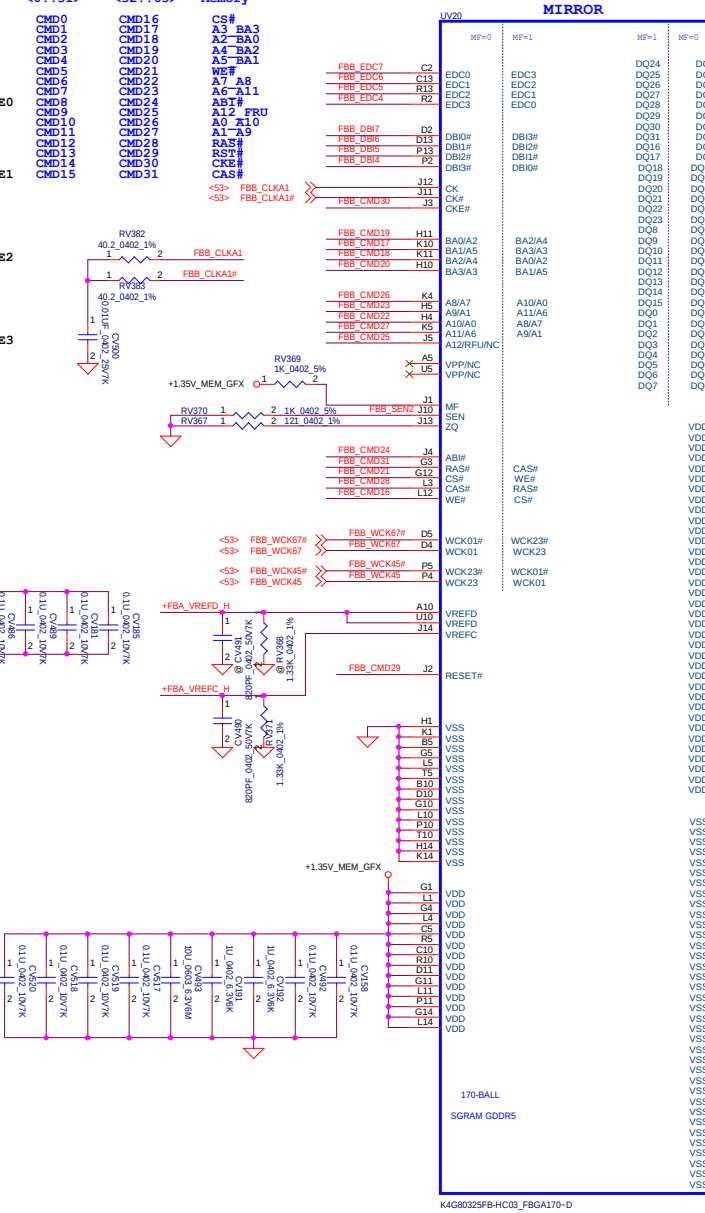


# GDDR5 CMD Mapping Table

<S3> FBB\_D[0..63] <<> FBB\_D[0..63]  
 <S3> FBB\_EDC[0..7] <<> FBB\_EDC[0..7]  
 <S3> FBB\_DB[0..7] <<> FBB\_DB[0..7]  
 <S3> FBB\_CMD[0..31] <<> FBB\_CMD[0..31]



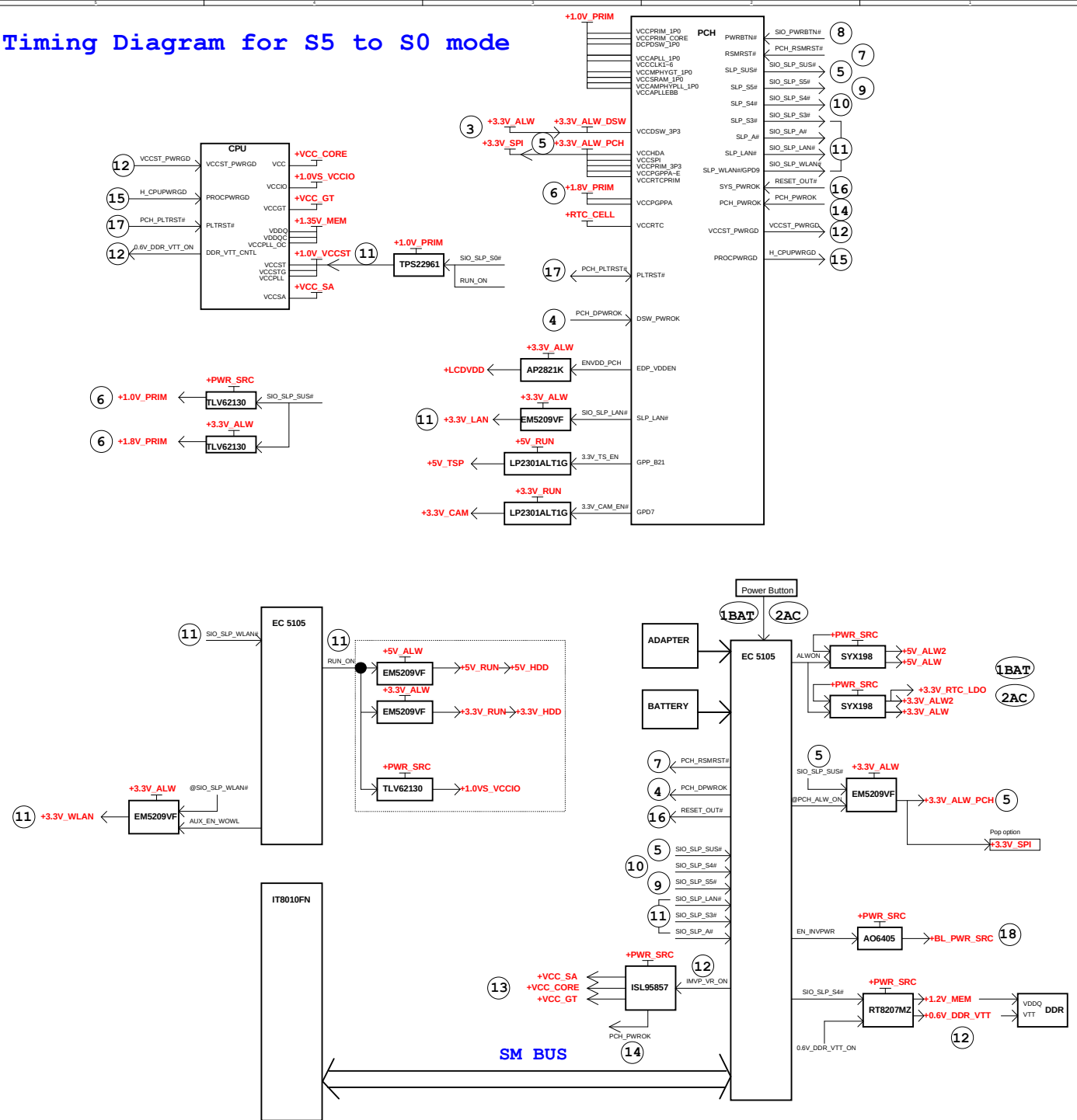
<0..31> <32..63> Memory  
 CMD0 CMD16 CS#  
 CMD17 A3 BA3  
 CMD18 A7 BA0  
 CMD19 A4 BA2  
 CMD20 A5 BA1  
 CMD21 WE#  
 CMD22 A7 A8  
 CMD23 A6 A11  
 CMD24 A8 A  
 CMD25 A12 FRU  
 CMD26 A0 A10  
 CMD27 A1 A  
 CMD28 RAS#  
 CMD29 RST#  
 CMD30 CK#  
 CMD31 CAS#



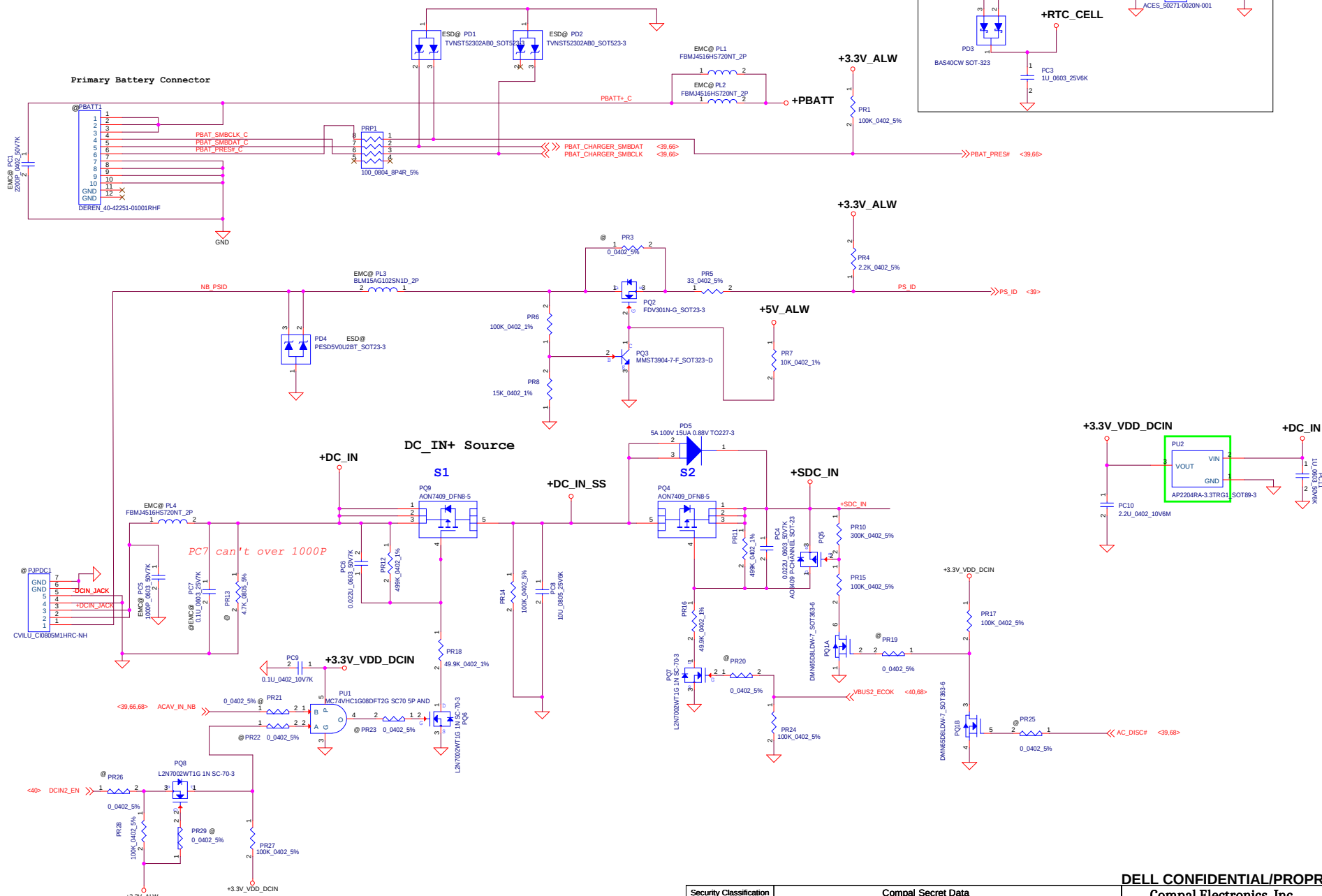
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GDDR5 VRAM B				Size
LA-E152P				Document Number
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### Timing Diagram for S5 to S0 mode

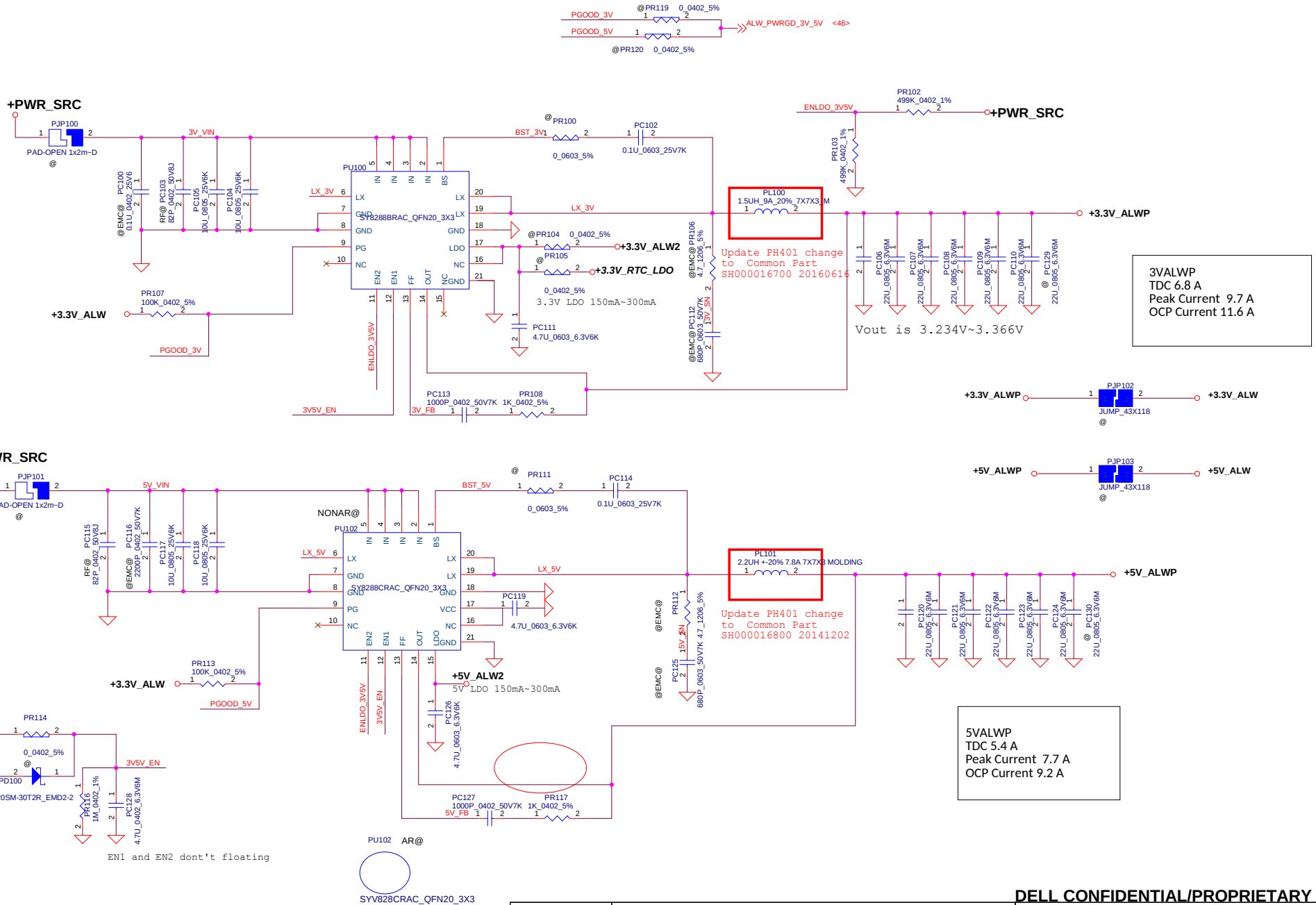






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		Size		Document Number	
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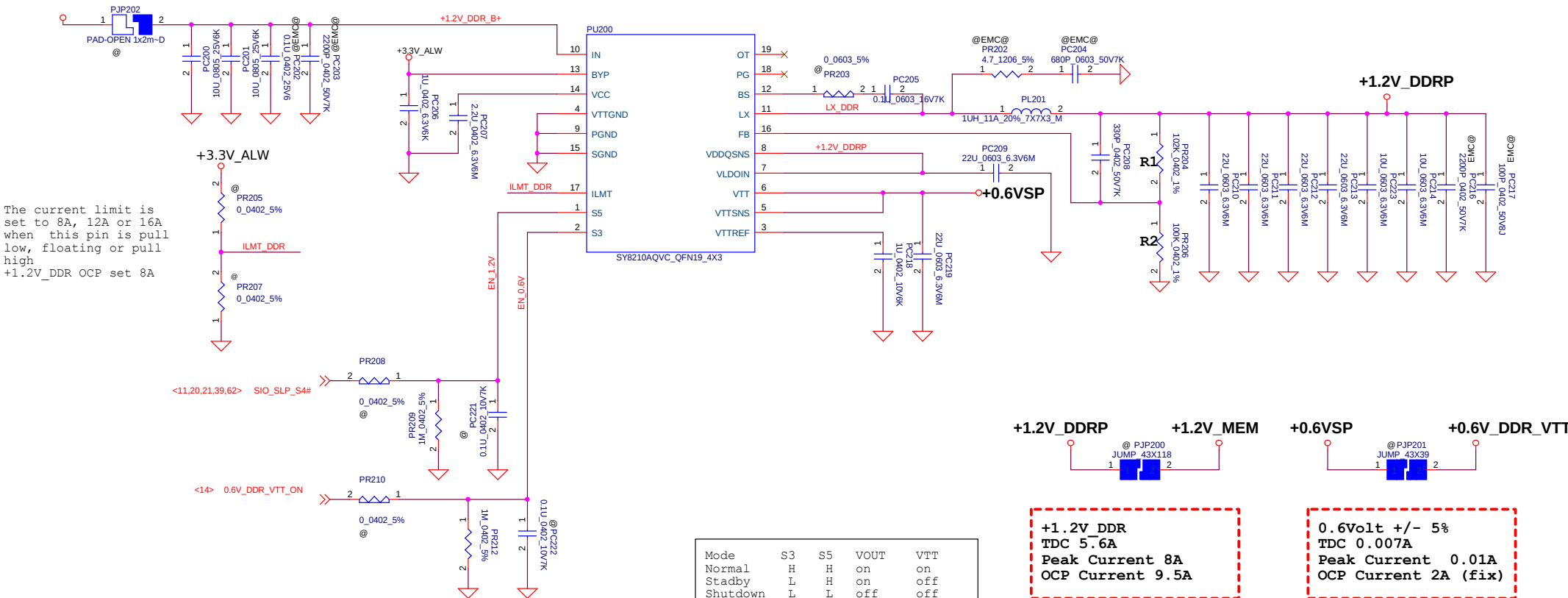




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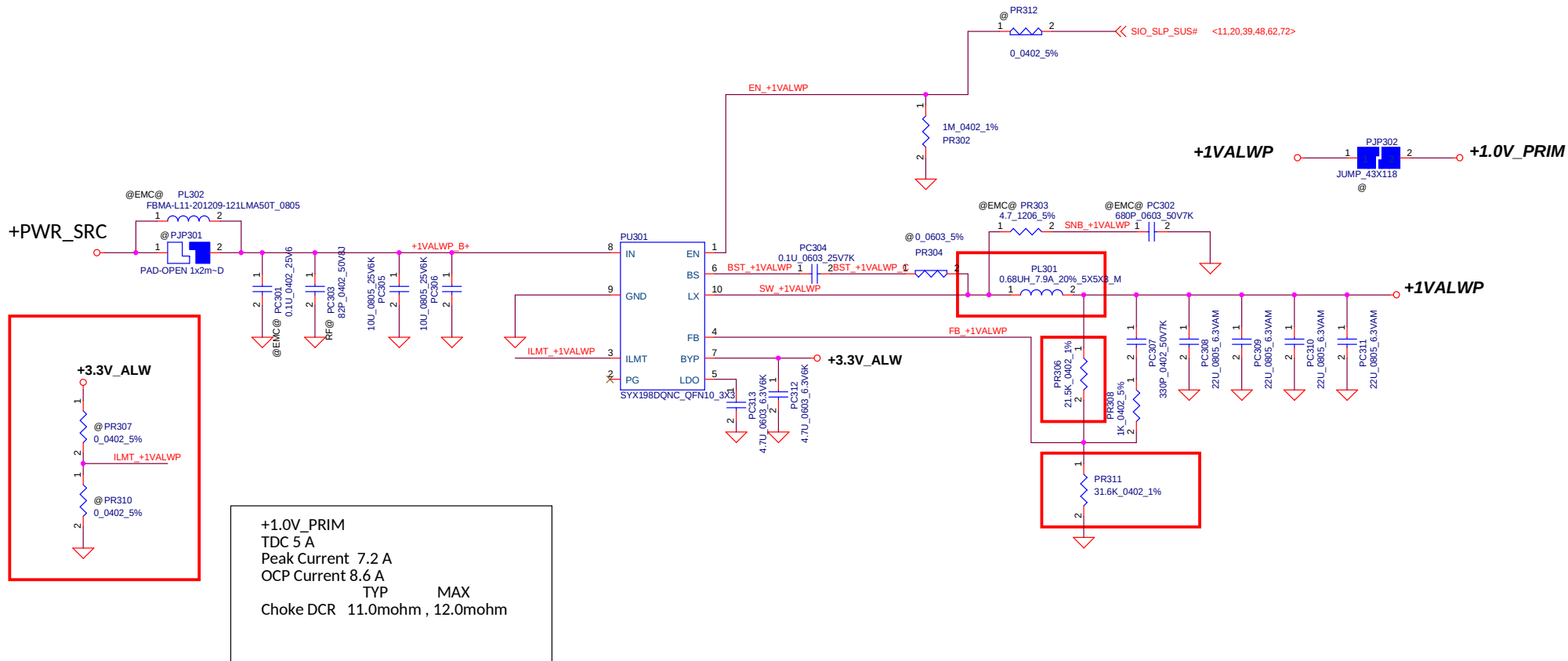


# +PWR\_SRC



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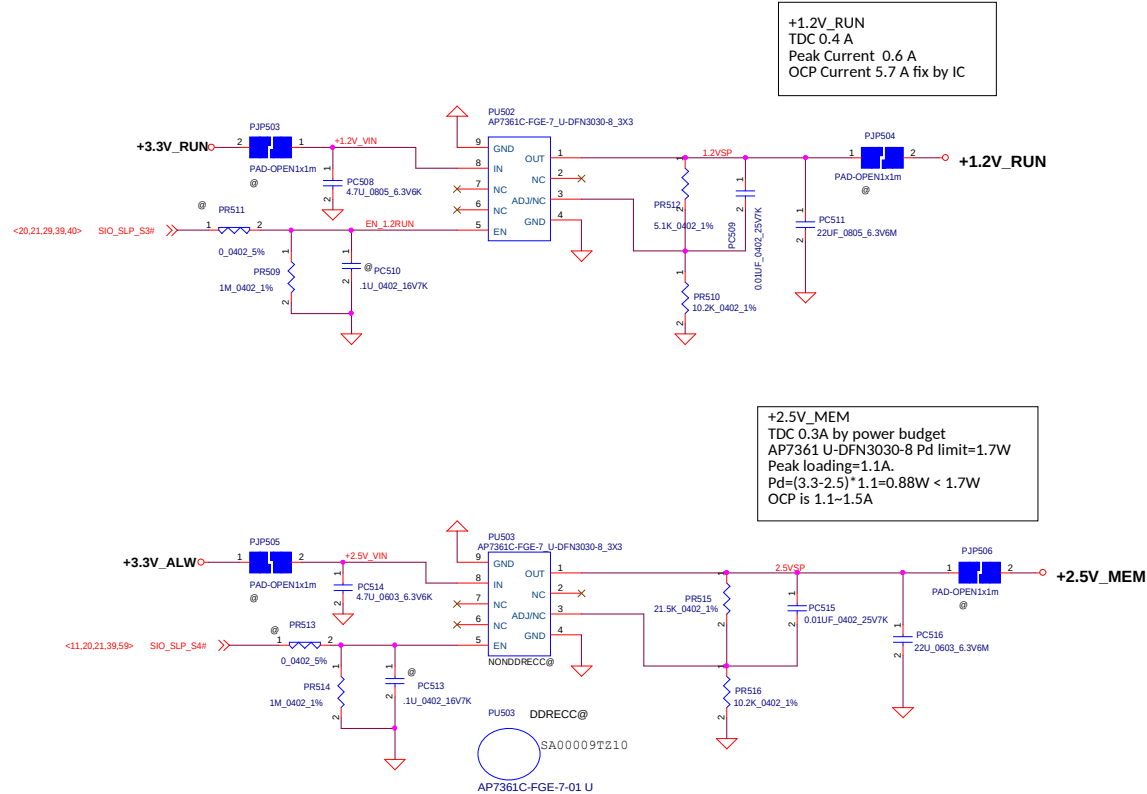
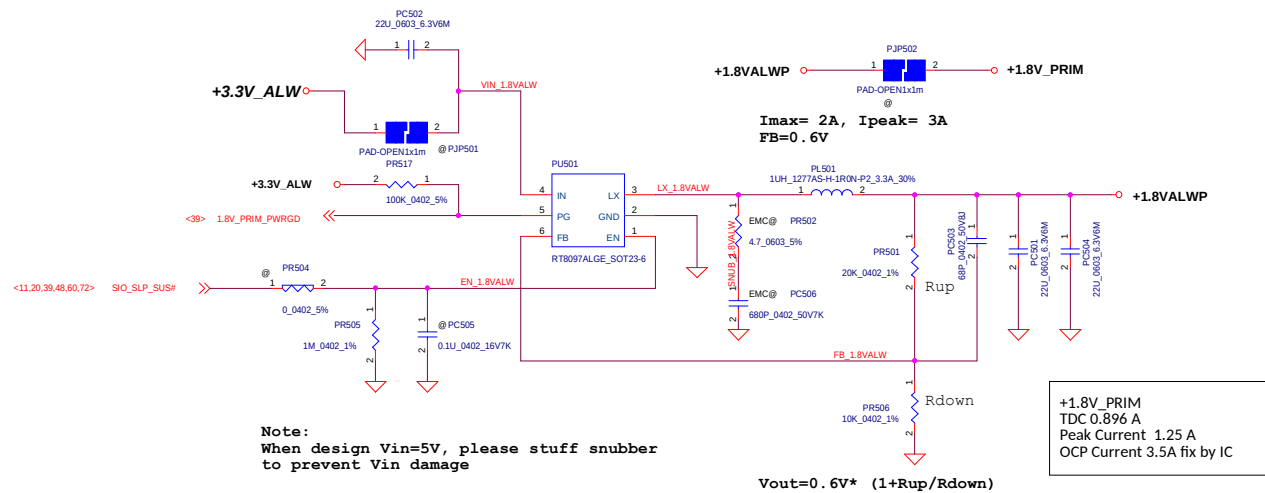
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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										+1VALWP	
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										74	
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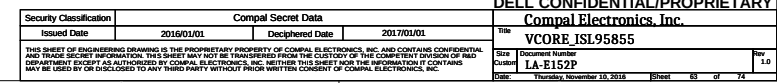


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+1.8VALWP/+1.5VSP/2.5V_MEN		
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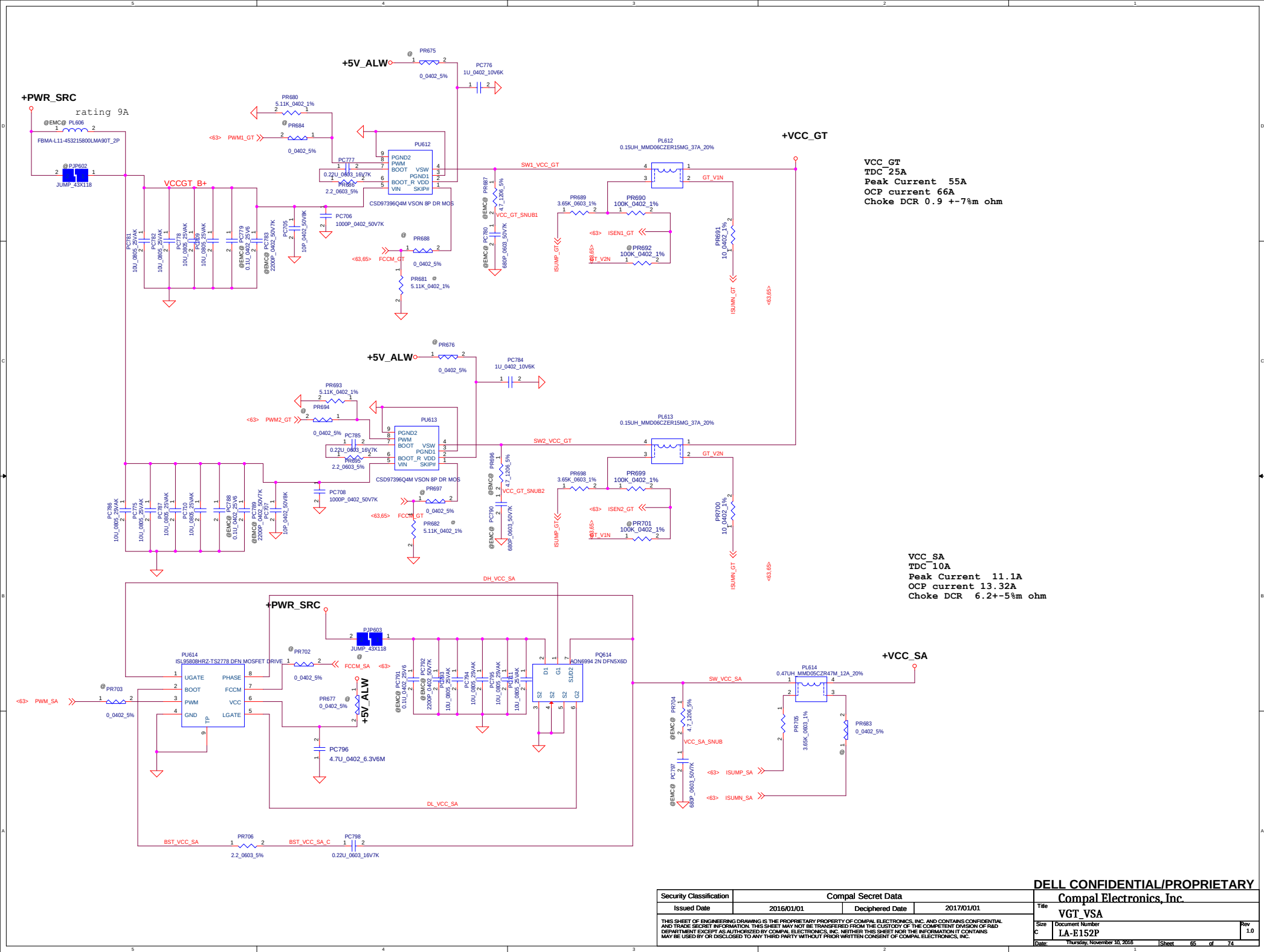












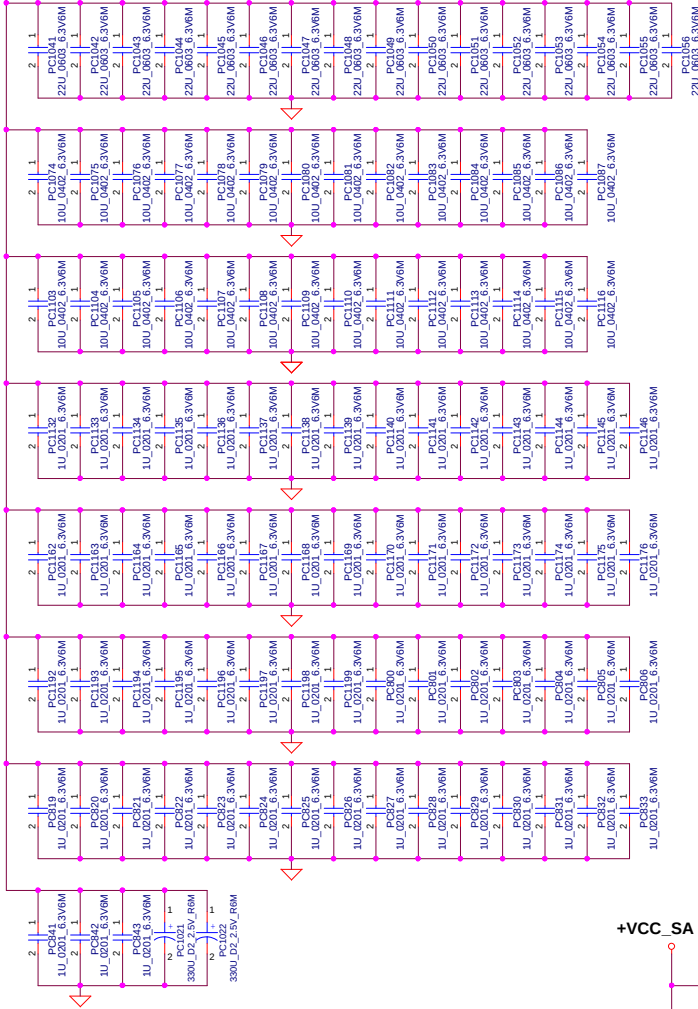






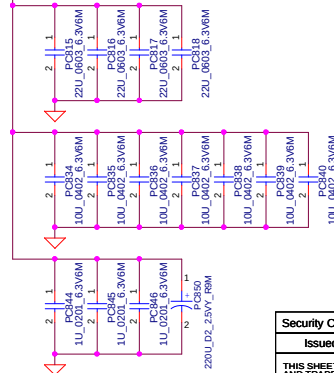
VCC CORE Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs + 10U\_0402\*28 pcs + 1U\_0201\*35 pcs  
Primary Side.  
22U\_0603 \* 8 pcs+330u\_D2\*2 pcs

+VCC\_CORE



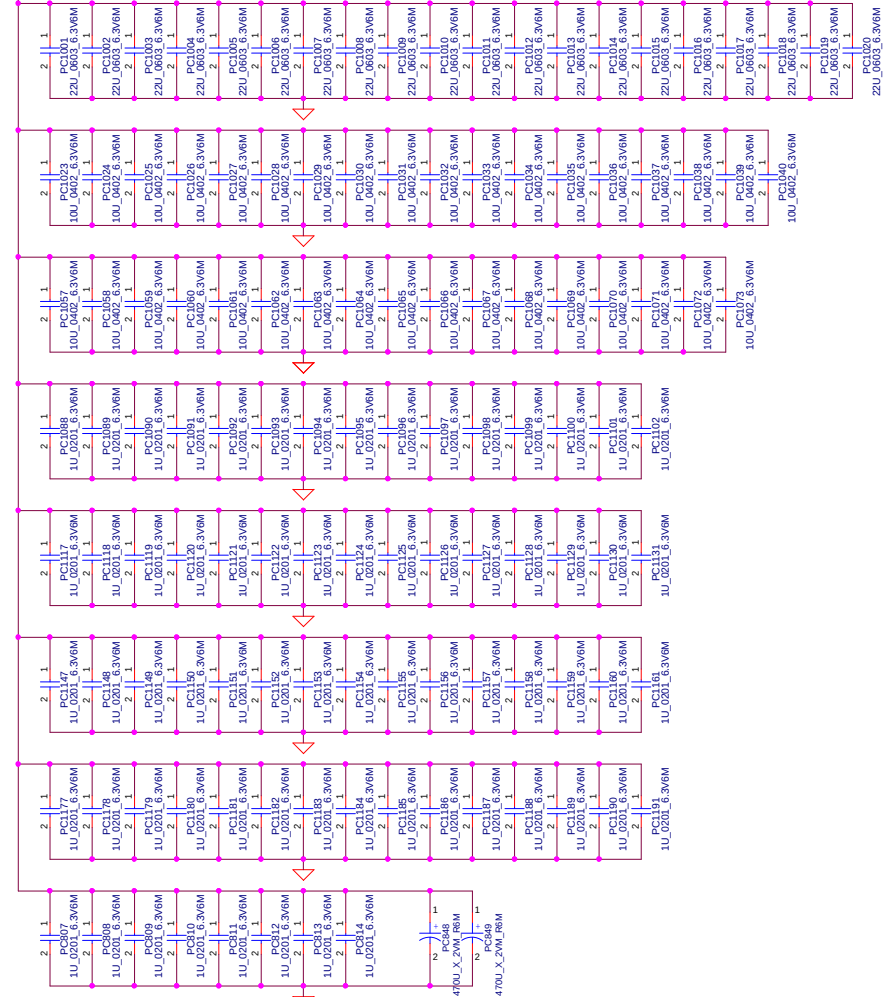
VCC SA Place on CPU  
Back Side.  
22U\_0603 \* 2 pcs + 10U\_0402\*7 pcs + 1U\_0201\*3 pcs  
Primary Side.  
22U\_0603 \* 2 pcs + 220u\_D2\*1 pcs

+VCC\_SA



VCC GT Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs +10U\_0402\*35 pcs +1U\_0201\*68 pcs  
Primary Side.  
22U\_0603 \* 12 pcs +470u\_D2\*2 pcs

+VCC\_GT



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$V_{boot} = V_{ref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$   
 $R = R_{refad} // (R_{boot} + R_{ref2})$   
 $V_{min} = V_{ref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R / (R_{ref1} + R)]$   
 $V_{max} = V_{ref} * R_{ref2} / [(R_{ref1} / R_{refad}) + R_{boot} + R_{ref2}]$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

#### PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of steps		96	96	20
Rrefad	PR9	39K	20K	39K
Rref1	PR5	39K	20K	30K
Rboot	PR8	1.5K	2K	3K
Rref2=PR10+PR12	PR10	30K	18K	24K
	PR12	1.5K	0	3K
C	PC8	1.5nf	2.7nf	1.8nf

**Module model information:**  
**RT8813A\_V1A for IC module**  
**RT8813A\_V1B for SW module**

PWM VID and Output voltage control  
 1. Boot mode  
 2. Standby mode (don't support)  
 3. Normal mode

Current Limit threshold setting  
 $R_{ocsc} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10uA$

$I_{ripple} = (19-0.9) * 0.9 / (304.89KHz * 0.36uF * 19) = 7.811A$

$OCP = 54A / 2 = 27A$  per phase  
 $I_{valley} = 27A - 7.811A / 2 = 23.1A$

H-side MOS:TPCA8065  
 $R_{ds(on)} = 11.7m\Omega @ V_{gs} = 10V$   
 $9.4m\Omega @ V_{gs} = 4.5V$   
 $I_d: 16A @ T_a = 25 \text{ degC}$

L-side MOS:TPCA8057  
 $R_{ds(on)} = 2.0m\Omega @ V_{gs} = 10V$   
 $2.6-3.2m\Omega @ V_{gs} = 4.5V$   
 $I_d: 42A @ T_a = 25 \text{ degC}$

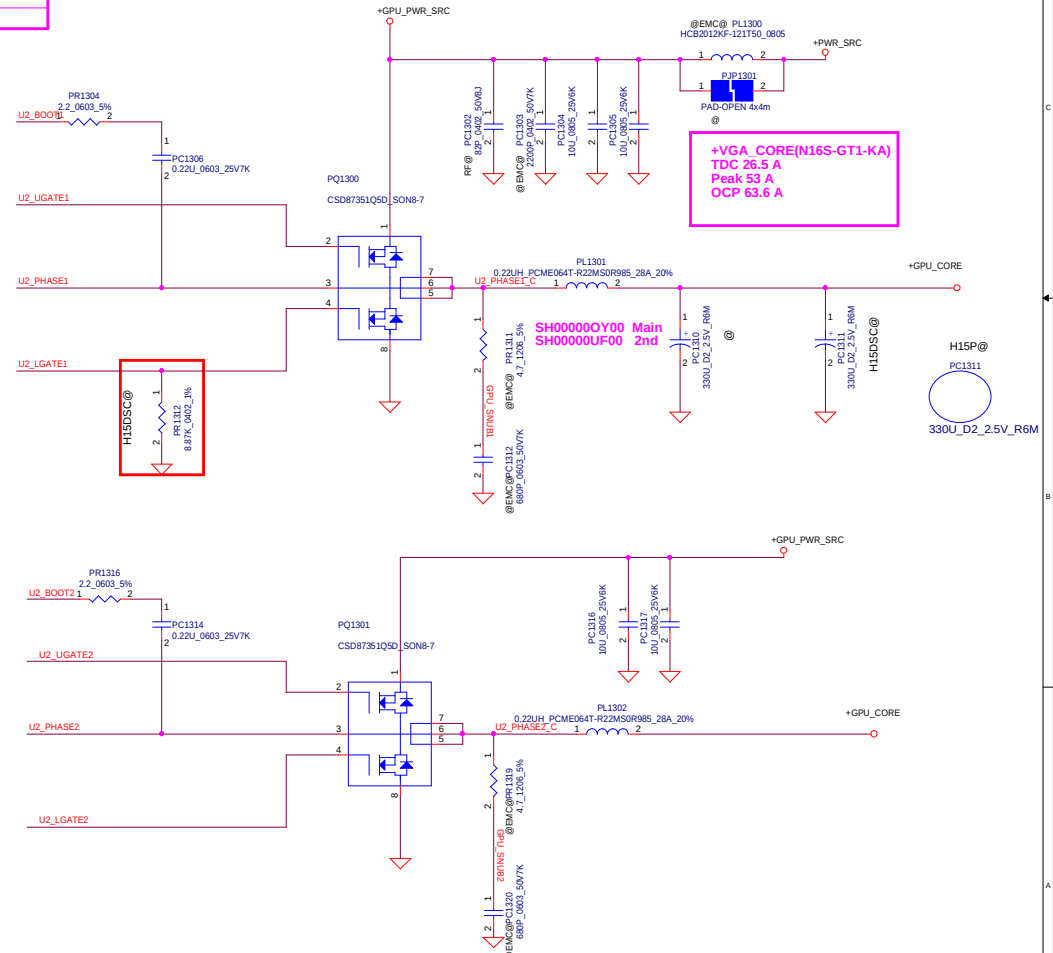
Choke: 0.36uH (Size:10\*10\*4)  
 $R_{dc} = 1.1m\Omega @ +5\%$   
 Heat Rating Current=30A  
 Saturation Current=50A

$C = 3 * 330uF (9m\Omega) = 990uF$   
 $V_{ripple} = I_{ripple} * ESR(\min) = 7.811A * 3m\Omega = 23.4mV$

Parameter	Value
Switching phase	180°
Load regulation	±0.5%
Line regulation	±0.5%
Temperature regulation	±0.5%
Power dissipation	10W
Operating temperature	0~70°C

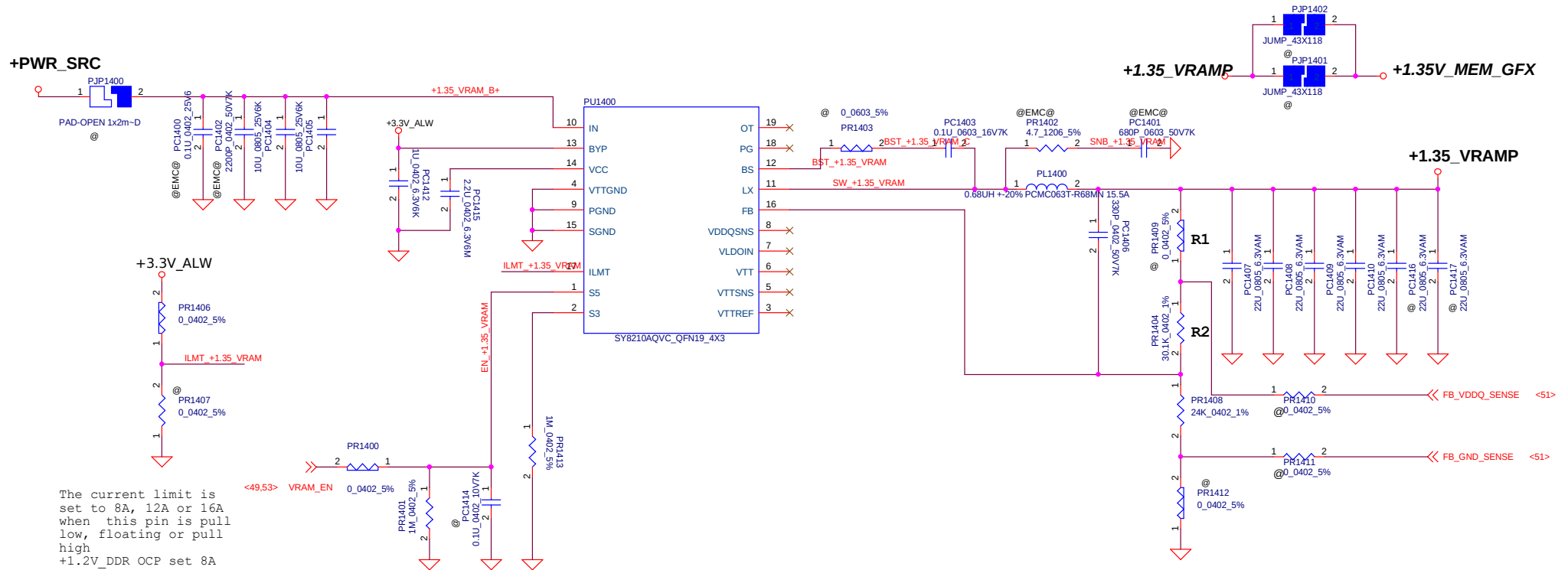
Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
Operating Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Power at Tj=100C	25W	32W	25W	20W	23W	N/A	30W	40W
Maximized GPU Total at Tj=100C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Continuous at Tj=100C	35A	55A	45A	35A	35A	40A	60A	75A
EDP-Peak at Tj=100C	15A	27A	25A	20A	14A	12A	31.5A	35A
Isleap max (Evaluation)	42A	66A	54A	42A	42A	48A	72A	90A
OCF Setting	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Current Rocset	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	8mohm * 3	8mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL





+PWR\_SRC



+1.35\_VRAM  
TDC 9A  
Peak Current 12A  
OCP Current 14.4A

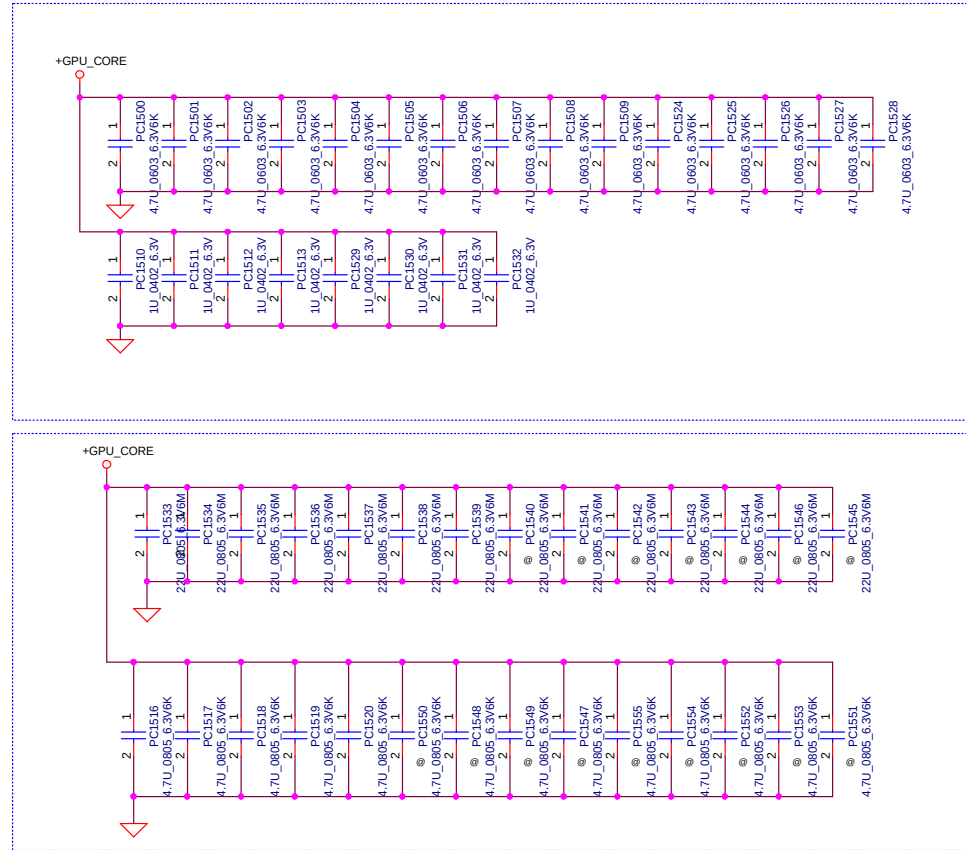
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GPU\_VRAM(SYX198D)

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nVidia GB4B-128 package  
Under GPU  
4.7uF 0603 \* 15  
1uF 0402 \* 8

nVidia GB4B-128 package  
Near GPU  
22uF 0805 \*7  
4.7uF 0805 \*5

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# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																										
	63				CPU VR controller change to 95855a ver. Support C10	PU601 to SA0000A4C00 from SA000082P2L	X00																										
1	68				Change the S4 fast turn off circuit to avoid the leakage.	TypeC: Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN.	X01																										
2	66 68				Add the Circuit for Multiple Input Detach detection & PROCHOT#	Charger: Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND. Add 1 net PROCHOT#_ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01																										
3	68				For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	TypeC: PR1219 change from 22.6K to 23.2K. SD034232280	X01																										
4	64 65				Location Alignment	H-Line VCCSA change the PU607 to PU614 and PL609 to PL614 and PQ601 to PQ614 IA change the PU602,603 to PU610,611 and PL603,604 to PL610,611 GT change the PU605,606 to PU612,613 and PL607,608 to PL612,613	X01																										
5	66				To decrease the charger input leakage voltage for TypeC AC.	Change the PD903 from SCS0340L010 to SCS00006C00.	X01																										
6	57 68				To solve the MOS leakage problem to avoid the error active.	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X01																										
7	68				Reserve the OVP function to protect the typeC device.	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205, PC1213, PC1214 and PR1248 Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm Re-modify the S11 OVP description to S3 OVP.	X01																										
8	63				CPU transient fine tune.	PC601 to 0.22uf_0402 from 0.33uf_0402 PC609 to 1000p from 680p PR640 to 115k from 110k PC624 to 820p from 330p	X01																										
9	58,60,69 66				EMI & RF request	RF:PC103 PC303 PC115 PC1302 pop 82P_0402 EMI: PR923 pop 4.7ohm, pc940 pop 680pf PR924 pop 4.7ohm pc941 pop 680pf PR914 to 3.3ohm from 0 ohm PR921 to 4.7 ohm from 2.2 ohm	X01																										
10	66				Charger IC version change from A to B version.	PU901 to SA00009VW20 from SA00009VW10	X01																										
11	69				VGA PG pull up R change to PWR from HW side.	Add VGA pull up PR1322 10K_0402	X01																										
12																																	
13																																	
14																																	
						<div>DELL CONFIDENTIAL/PROPRIETARY</div> <table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Title</td></tr><tr><td>Issued Date</td><td>2016/01/01</td><td>Deciphered Date</td><td>2017/01/01</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td colspan="4" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td colspan="2">PWR P.I.R</td></tr><tr><td colspan="2">LA-E152P</td></tr><tr><td colspan="4">Date:</td><td colspan="2">Thursday, November 10, 2016</td></tr></table>		Security Classification	Compal Secret Data			Title		Issued Date	2016/01/01	Deciphered Date	2017/01/01	Compal Electronics, Inc.		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR P.I.R		LA-E152P		Date:				Thursday, November 10, 2016	
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Version Change List ( P. I. R. List )							
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	2016/5/27	COMPAL	Change Panel ID setting for RM15P.	Change RM330 from 33k to 4.3k. (SD028483180)	0.2 (X01)
2	11	HW	2016/5/27	COMPAL	Stuck(morden standy) support for VCCPLA_OC	Pop RE122 and depop U614	0.2 (X01)
3	39	HW	2016/5/27	COMPAL	Reserve PORT90_DET8 PD resistance	Add Rst.Usms VCCPVD_RM(U619.4) and connect to RE120.1	0.2 (X01)
4	37	HW	2016/6/1	COMPAL	Intel schematics review modify item	Reserve RM513 100k (SD028100380) to GND	0.2 (X01)
5	47	HW	2016/6/1	COMPAL	J1801 pin definition error	CE28,CE29 change from 0.047uF to 0.01uF CV2 change from 1.0uF to 10uF 0603	0.2 (X01)
6	41	HW	2016/6/1	COMPAL	TMN change to MOVOTON	J1801 pin definition change	0.2 (X01)
7	37	HW	2016/6/1	COMPAL	Initial review result (WMM Core feature support)	Change TMN from Atmel to MOVOTON	0.2 (X01)
8	37	HW	2016/6/7	COMPAL	Debug card reserve	Add RE122 0 ohm connect WMM_CORE1 and WLAN_CORE1 Add RE122 0 ohm connect WMM_CORE2 and WLAN_CORE2 Add RE130 0 ohm connect WMM_CORE1 and WLAN_CORE1	0.2 (X01)
9	39	HW	2016/6/7	COMPAL	For MEC5105-01-TM setting	Add RE131, RE132 for PORT90_DET8 and HOST_DET8U_TX	0.2 (X01)
10	27	HW	2016/6/15	COMPAL	HEMT RA FAIL	1. Change USB to SA000091000 2. POP RM361,RE362 3. De-POP RM361	0.2 (X01)
11	29	HW	2016/6/15	COMPAL	Change AR crystal	Pop RV47, change RW to 1.6uH	0.2 (X01)
12	34,37	HW	2016/6/16	COMPAL	For BMC request	Change TT1 to S210000MC00.	0.2 (X01)
13	43	HW	2016/6/16	COMPAL	BIT0284924-RD0 is still working after press power button into BS during BOOT.	Depop RE133, RE139, CE22 change to 10uF, POP CA7,CE1 (100P),CE18 modify from 22p to 47p and POP.Change IY1 to SM01000W00	0.2 (X01)
14	27	HW	2016/6/17	COMPAL	For backdrive issue	POP RM5	0.2 (X01)
15	41	HW	2016/6/17	COMPAL	Connector change	Pop C10,PD0,RYW08,RY891 PD to +3.3V_ALM_P0S	0.2 (X01)
16	38	HW	2016/6/20	COMPAL	Vendor support	1. J1801 change to CV13D,CE1500P00000-05-WH 2. J1801 change to CV13D,CE1500P00000-05-WH 3. J1801 change to ACCE,SD000-06000-P01	0.2 (X01)
17	39	HW	2016/6/22	COMPAL	The possibility of GPIO map update	RV2,RA8 change to 14.2ohm	0.2 (X01)
18	43	HW	2016/6/22	COMPAL	Depop request	Add RE514,RE515 for MOVOTON	0.2 (X01)
19	38	HW	2016/6/28	COMPAL	XS have no difference J1801 pin define	FFE VDD_10 change to +3.3V_GND	0.2 (X01)
20	38	HW	2016/6/28	COMPAL	Let USB_Pwr_Status keep low at 45	Depop DS7,Pop RM87	0.2 (X01)
21	36	HW	2016/6/28	COMPAL	For RM1 Board ID	RT10 change from 3M to 100k ohm	0.2 (X01)
22	24	HW	2016/6/28	COMPAL	For VDA test result	RT79 change from 240k to 100k ohm	0.2 (X01)
23	21	HW	2016/6/28	COMPAL	For VDA test result	Pop RV121/RV122/CV133	0.2 (X01)
24	38	HW	2016/6/28	COMPAL	Vendor schematic review	CE, RM Change to 100k, RM Change to 100k De-POP RM346	0.3 (X02)
25	39	HW	2016/6/28	COMPAL	Vendor schematic review	1. Add net W0878 to UE2.4 and CE500 1uF (SD000000000) 2. Add RE523 0 ohm for USB power pin and start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 5. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 6. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 7. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 8. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 9. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 10. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 11. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 12. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 13. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 14. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 15. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 16. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 17. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 18. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 19. 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26	7	HW	2016/6/28	COMPAL	Initial suggestion	Change RE137 from 1k ohm to 3k ohm	0.3 (X02)
27	32	HW	2016/6/28	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3 (X02)
28	46	HW	2016/6/28	COMPAL	Touchpad IIC RA	Change RE20, RE21 from 4.7k ohm to 2.2k ohm Change CE80, CE81 from 330pF to 10pF	0.3 (X02)
29	31	HW	2016/6/28	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3 (X02)
30	42	HW	2016/6/28	COMPAL	Board ID	Change RT79 to 62kOhm (SD02805280)	0.3 (X02)
31	38	HW	2016/6/28	COMPAL	MC screw hole update	Change R11/R23 from 3.8 to 5.2mm	0.3 (X02)
32	45	HW	2016/6/28	COMPAL	DFB request	MC concern CE1, CE2, CE3, CE4 PCB pad is too small, easy to cause damage issue, request use the symbol "R55050H-3072S, SMC2-2" follow PCB	0.3 (X02)
33	45	HW	2016/6/28	COMPAL	OCV function error	POP RC314/RC315	0.3 (X02)
34	21	HW	2016/6/28	COMPAL	DDPU_PWR_EN need to use BIOS solution	DSC BOM change -> DGPU_PWR_EN De-POP RM349, POP RM346	0.4 (X03)
35	39	HW	2016/6/28	COMPAL	TMN change MPTC650V02TX	Change UE11 from SA00000RE170 to SA00000RE180	0.4 (X03)
36	38	HW	2016/6/28	COMPAL	Expander I/O change from ITE to Microchip MCP3108	Change UE2 from SA00000V200 to SA00000ADQ00, reserve RE523 Change RE524, RE525 from 10kOhm to 2.2kOhm	0.4 (X03)
37	37	HW	2016/6/28	COMPAL	Board ID	Change RT79 to 33kOhm (SD028330280)	0.4 (X03)
38	37	HW	2016/6/28	COMPAL	EC request for power consumption	Reserve RE526(10K) PD for USB DET8 to +3.3V_ALM Add RE525 PD for LAN cable DETCT8 (Reserve) Add RE526 PD for LAN cable DETCT8 (Reserve)	0.4 (X03)
39	39	HW	2016/6/28	COMPAL	USB/B depop, pop on MB side	POP RE18,RE9	0.4 (X03)
40	12,16	HW	2016/6/28	COMPAL	PD 1.0 update items	Change RT79 from 430hm to 330hm change RE60 from 430hm to 330hm,CC187,CC188,CC189,CC272 from 22uF to 10uF and De-pop CC272	0.4 (X03)
41	45	HW	2016/6/28	COMPAL	MC screw hole update	R17 change from H_398 to R_496	0.4 (X03)
42	38	HW	2016/6/28	COMPAL	Reserve two resistors for PCR_DPWROR circuit	Add RE536 and RE537 for resistors for PCR_DPWROR circuit	0.4 (X03)
43	37	HW	2016/6/28	COMPAL	MC issue fix options & assessment	pop RE361 / depop RE362	0.4 (X03)
44	36	HW	2016/6/28	COMPAL	BR audio RM1 issue	1. Add net W0878 to UE2.4 and CE500 1uF (SD000000000) 2. Add RE523 0 ohm for USB power pin and start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 5. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 6. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 7. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 8. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 9. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 10. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 11. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 12. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 13. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 14. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 15. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 16. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 17. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 18. Change RE14, RE15, RE18 from 100k ohm to 10k ohm 19. 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45	51	HW	2016/6/28	COMPAL	Fix turn MV power sequence	CV241 change from 3300uF to 4700uF (SD074471880) CV248 change from 220uF to 470uF (SD074471880)	0.4 (X03)
46	38	HW	2016/6/28	COMPAL	BIT0294007-Sometimes need to press power button twice to power on system	Change CE12 to 2.2uF and RE33 to 10kOhm	0.4 (X03)
47	27	HW	2016/6/28	COMPAL	SD of HYVINC RA can pass	De-POP RV121/RV122	0.4 (X03)
48	29	HW	2016/6/28	COMPAL	For VI PD Controller RSD issue	CT85,CT86 change from 220p to 470p.(SD074471880)	0.4 (X03)
49	38	HW	2016/11/01	COMPAL	EC watchdog reserve	Add Q13,RE330,CE503	1.0 (X04)
50	38	HW	2016/11/01	COMPAL	Board ID change to A50	Change RT79 to 4.3k ohm(SD028430180)	1.0 (X04)
51	37	HW	2016/11/01	COMPAL	UE1.R8 to prevent EOS issue on MEC5105	Add RE519(100ohm) to CV2_0N	1.0 (X04)
52	32,41,46	HW	2016/11/01	COMPAL	Depop Maxim RS Component	Depop UE25 group parts.	1.0 (X04)
53	33	HW	2016/11/01	COMPAL	Change Intel PHY R/N SA000008011 for HP part	Change Intel PHY R/N SA000008011 for HP part	1.0 (X04)
54	20,21	HW	2016/11/01	COMPAL	For DFB request.	Close solder mask CM051 (-WMM) and other co-layer part	1.0 (X</